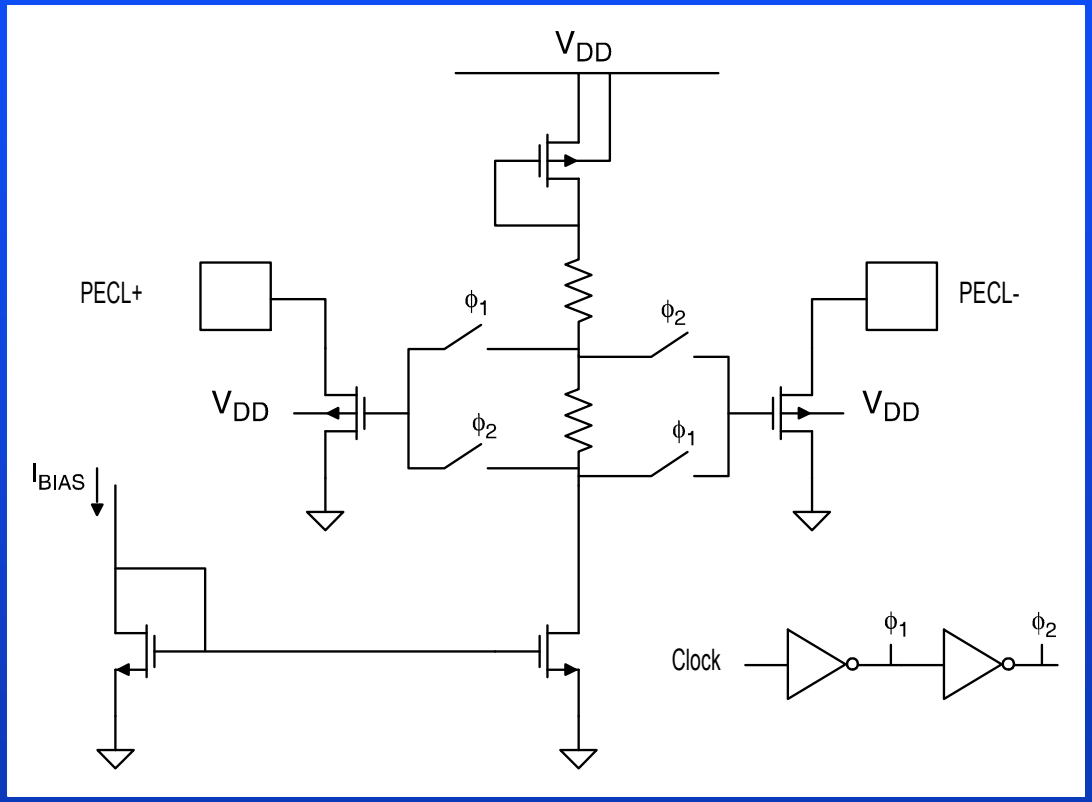
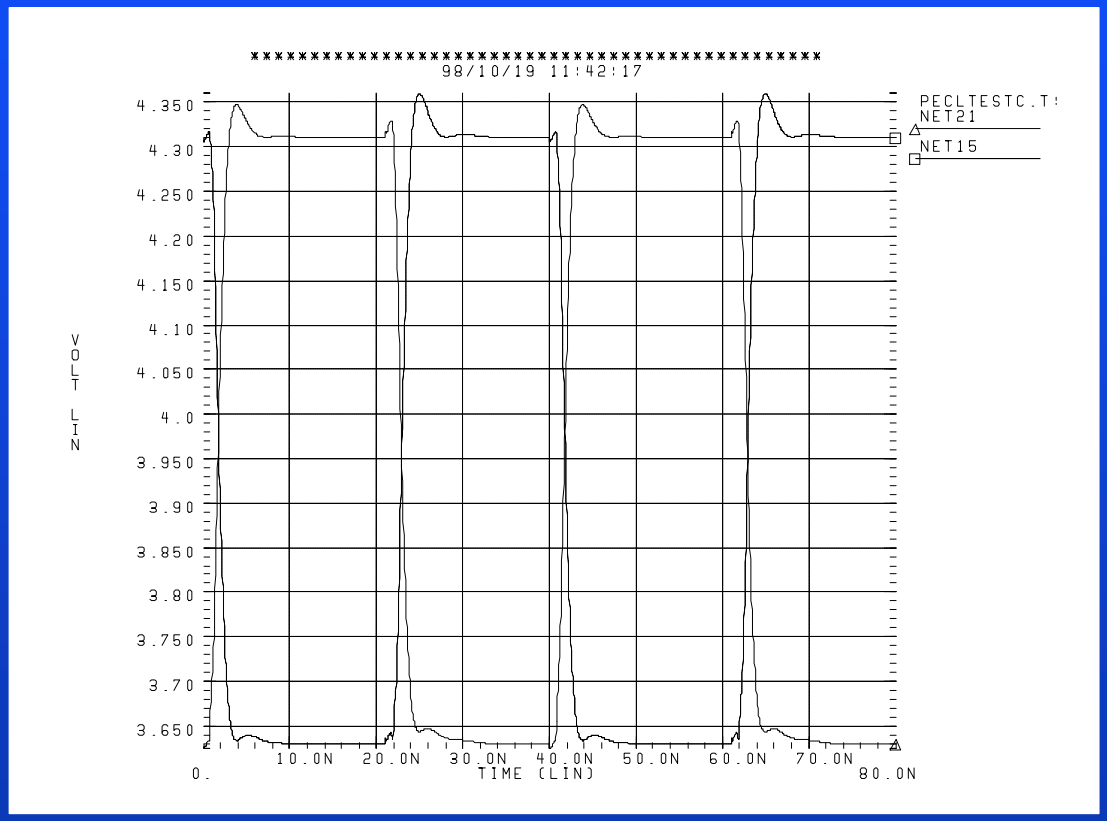
Successful Design Looks Beyond the Schematic

PECL in a PICKLE

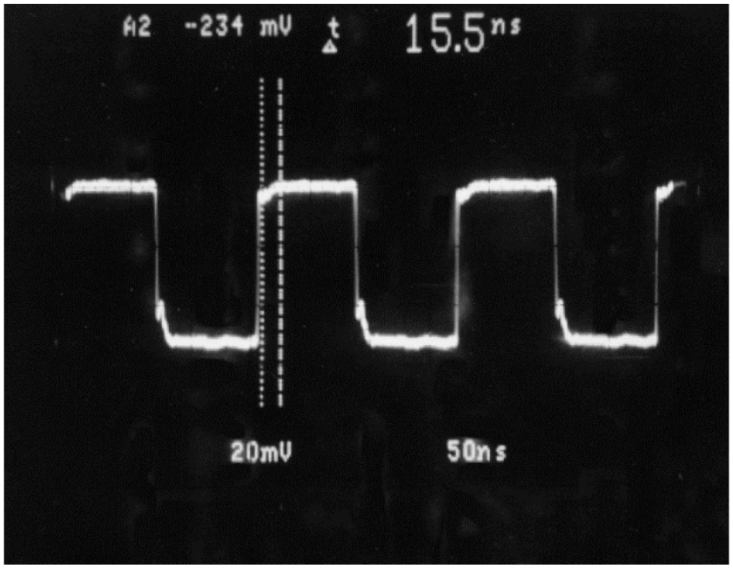
Pseudo ECL Driver (PECL) Schematic

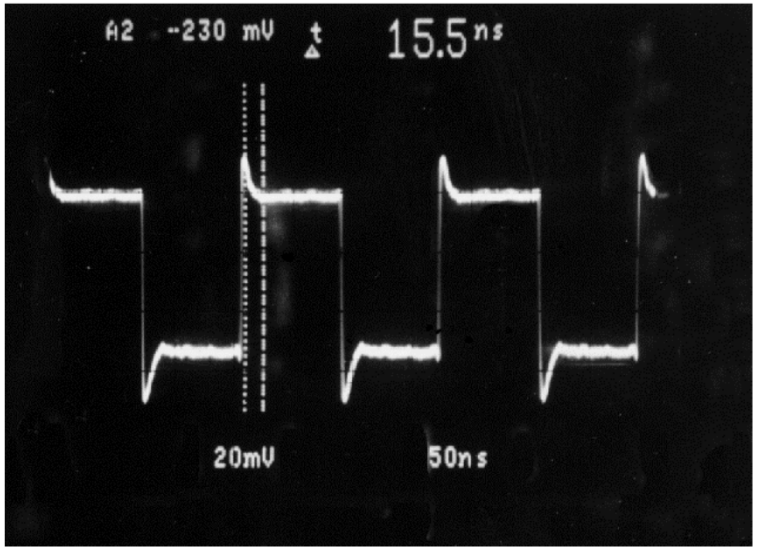


PECL Output Simulations: SPICE from Schematics



PECL Outputs in Silicon





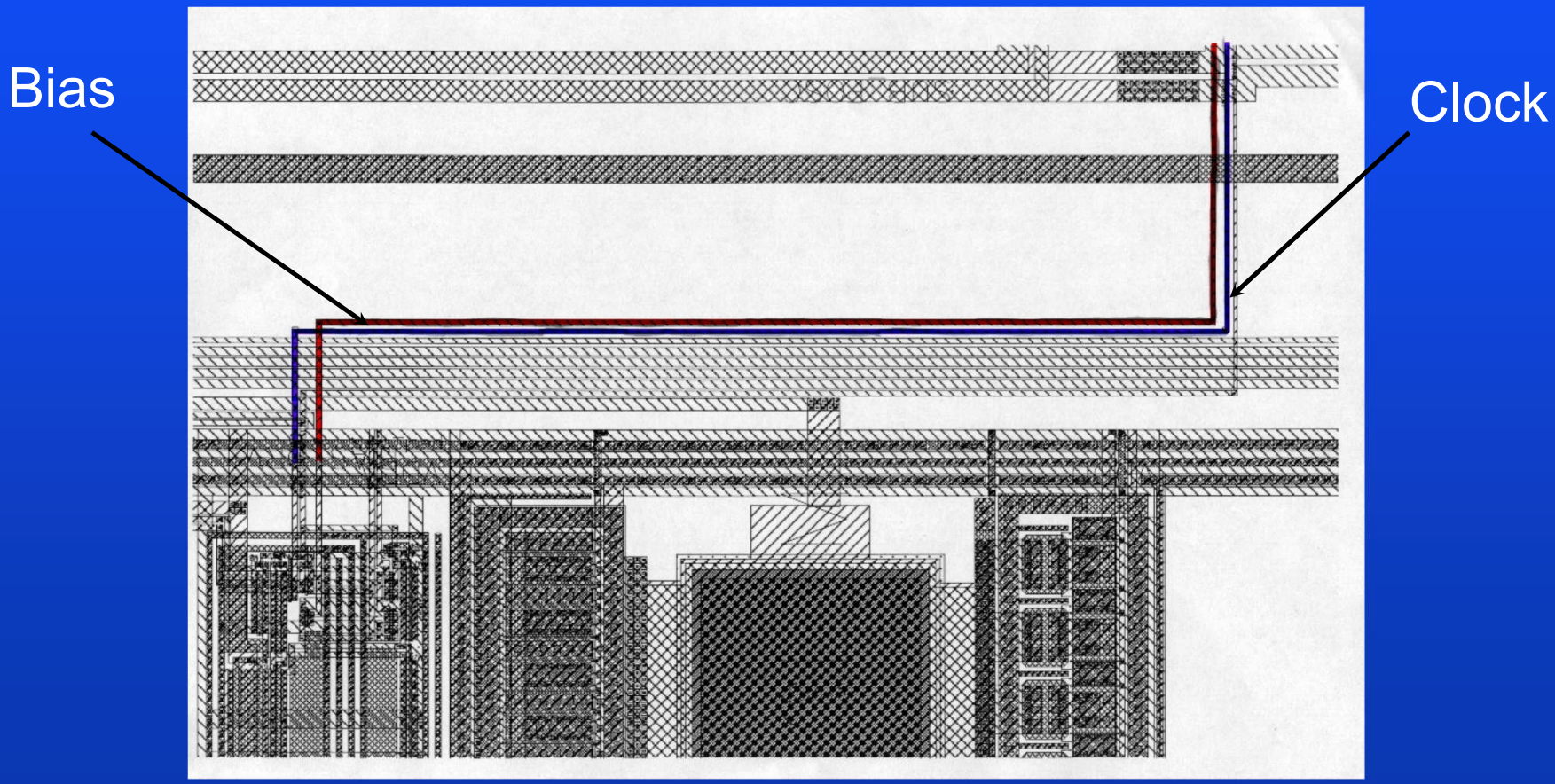
BAD

What went wrong???

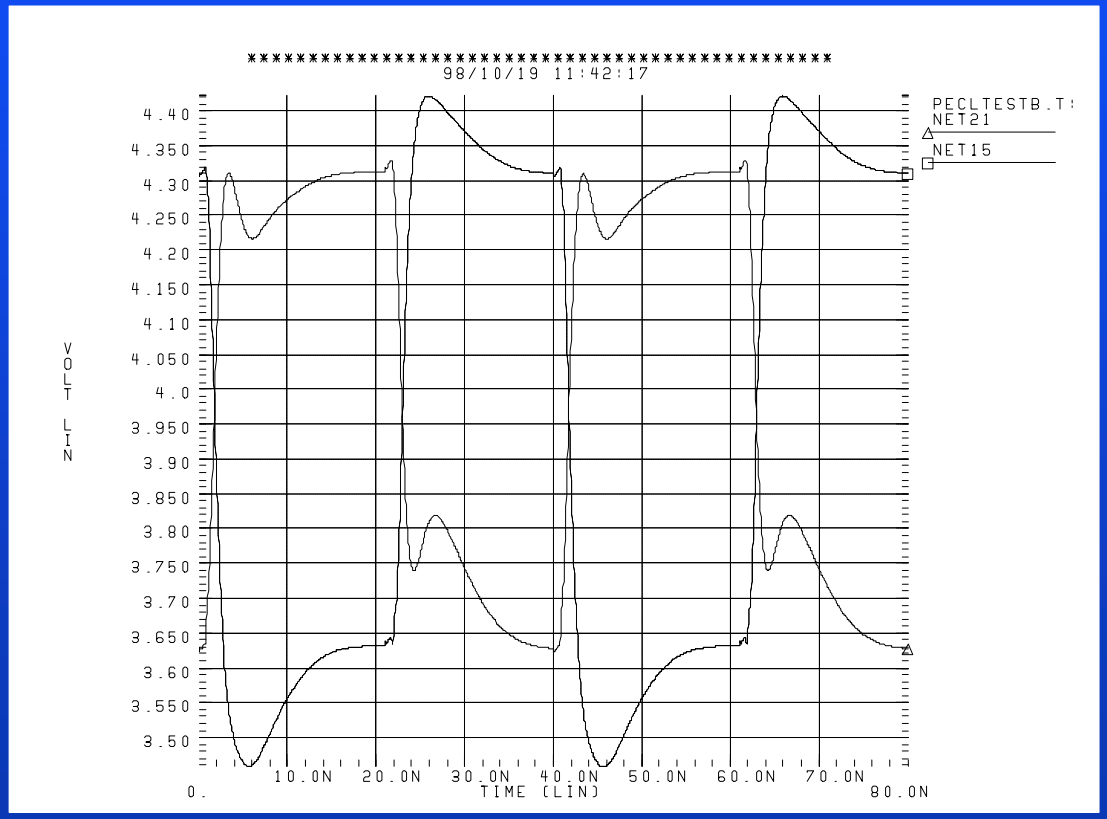
Candidate Answers

- SPICE
- SPICE Models
- Charge feedthrough from switches
- Package lead inductance
- Package interlead mutual inductance
- Some other parasitic??

Layout of PECL Bias and PECL input Clock



PECL Output with 5fF coupling!!



Lessons Learned

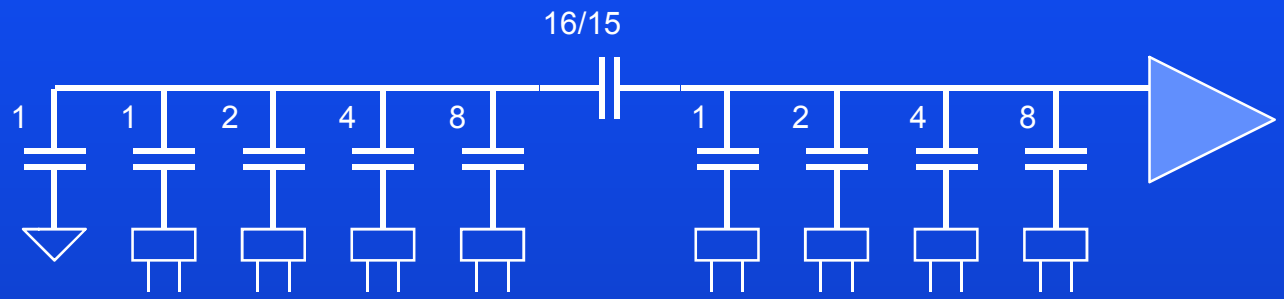
- **TAKE CARE WITH ALL BIAS LINES!**
  - **Shield them from stuff below**
  - **Shield them from stuff above**
  - **Shield them from stuff beside**

How small is small?

A 8-Bit SAR Case Study

- **Description**
  - **8-Bit SAR A/D Converter**
  - **0.35μm CMOS Double-Poly, Quad Metal**
  - **Array used "bridge capacitor" technique**
  - **Unit Capacitor was ~48 fF (7μm x 7μm)**

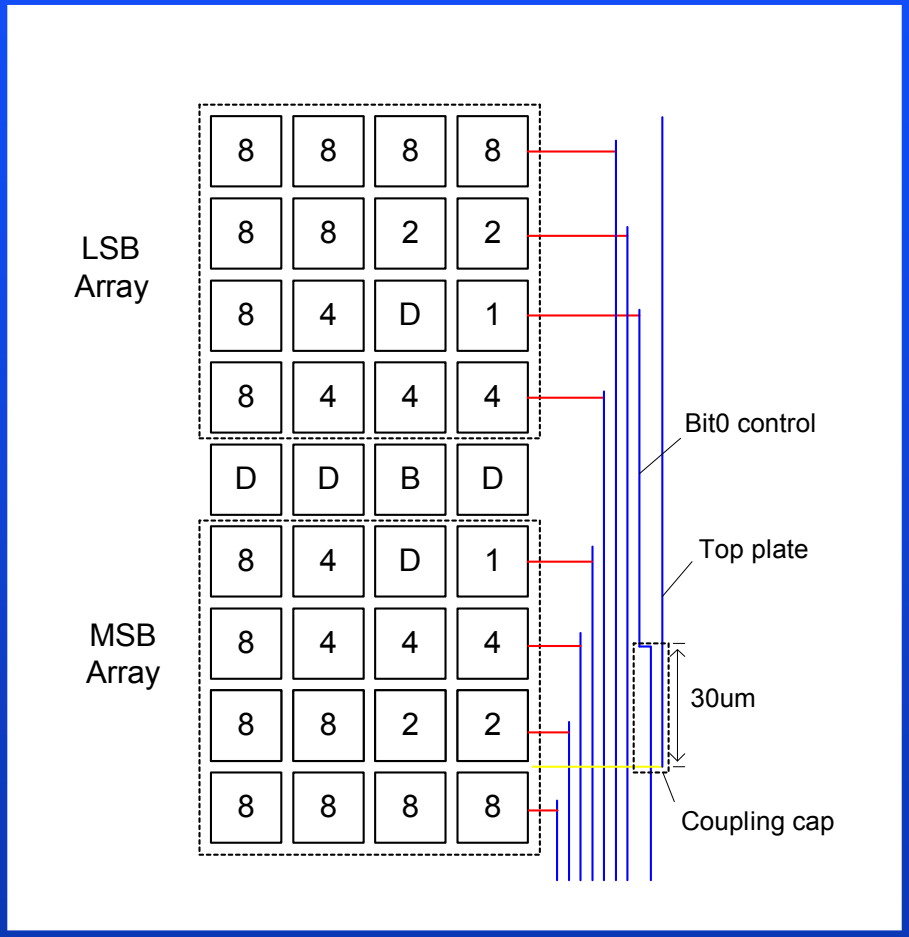
8-Bit Capacitor Array



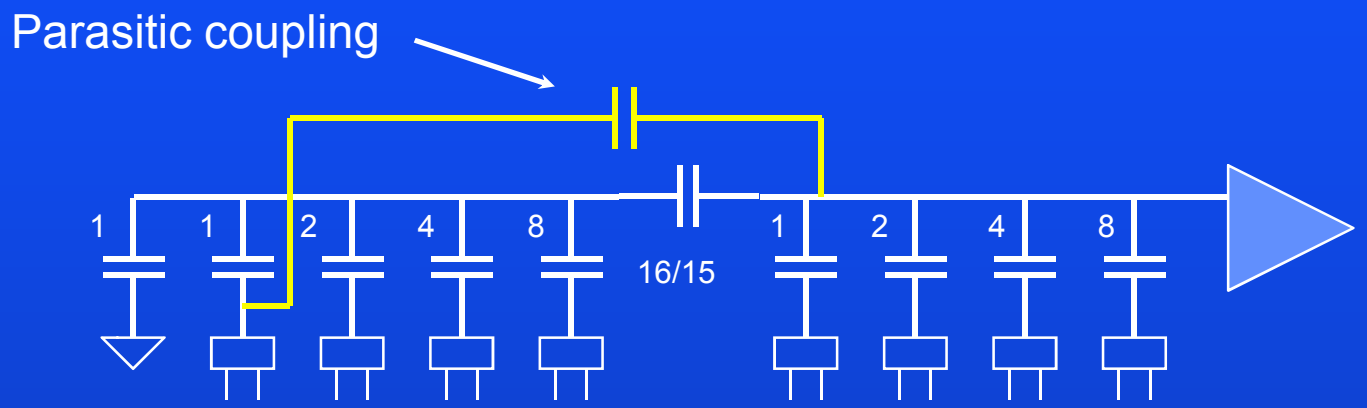
Unit capacitor is 48 fF

Capacitor Array

View shows top plate only



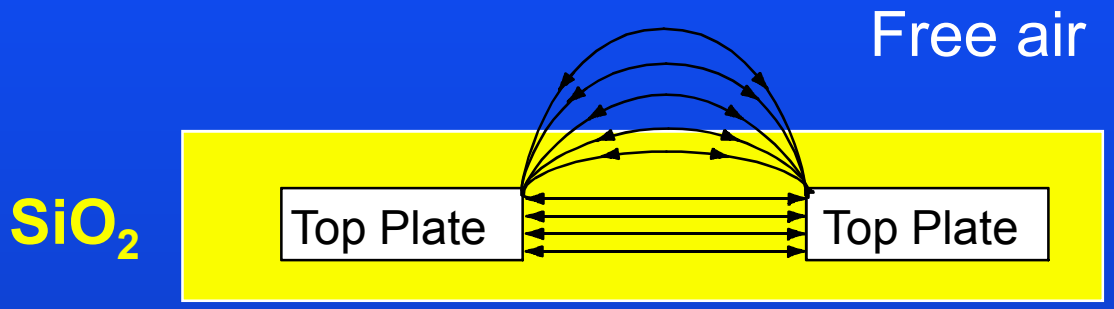
Capacitor Array



Parasitic coupling is MAGNIFIED across the bridge capacitor and thus for 48 fF unit capacitors a 3 fF parasitic coupling capacitor is magnified by 16! This DOUBLES the weight of Bit0!!! Thus 3fF changes an 8-bit converter to a 7-bit converter.

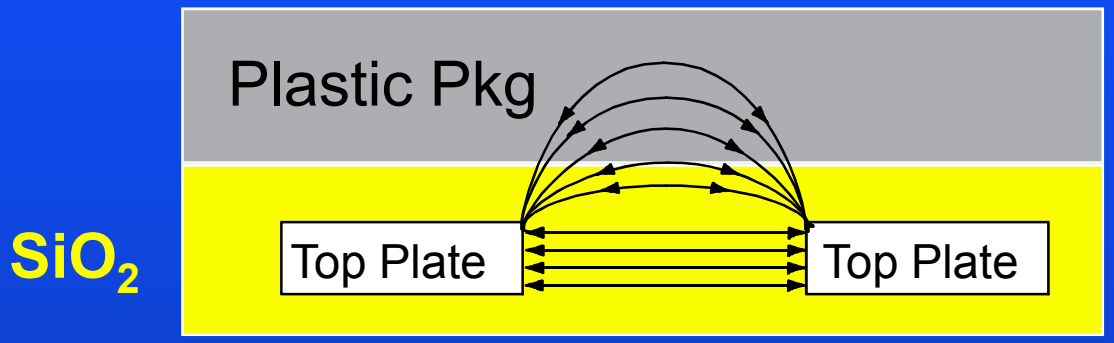
Does Plastic Change Your Life?

Coupling Varies with Dielectric



Before plastic encapsulation, the fringe extends into free air ($\varepsilon \sim 1$)

Coupling Varies with Dielectric



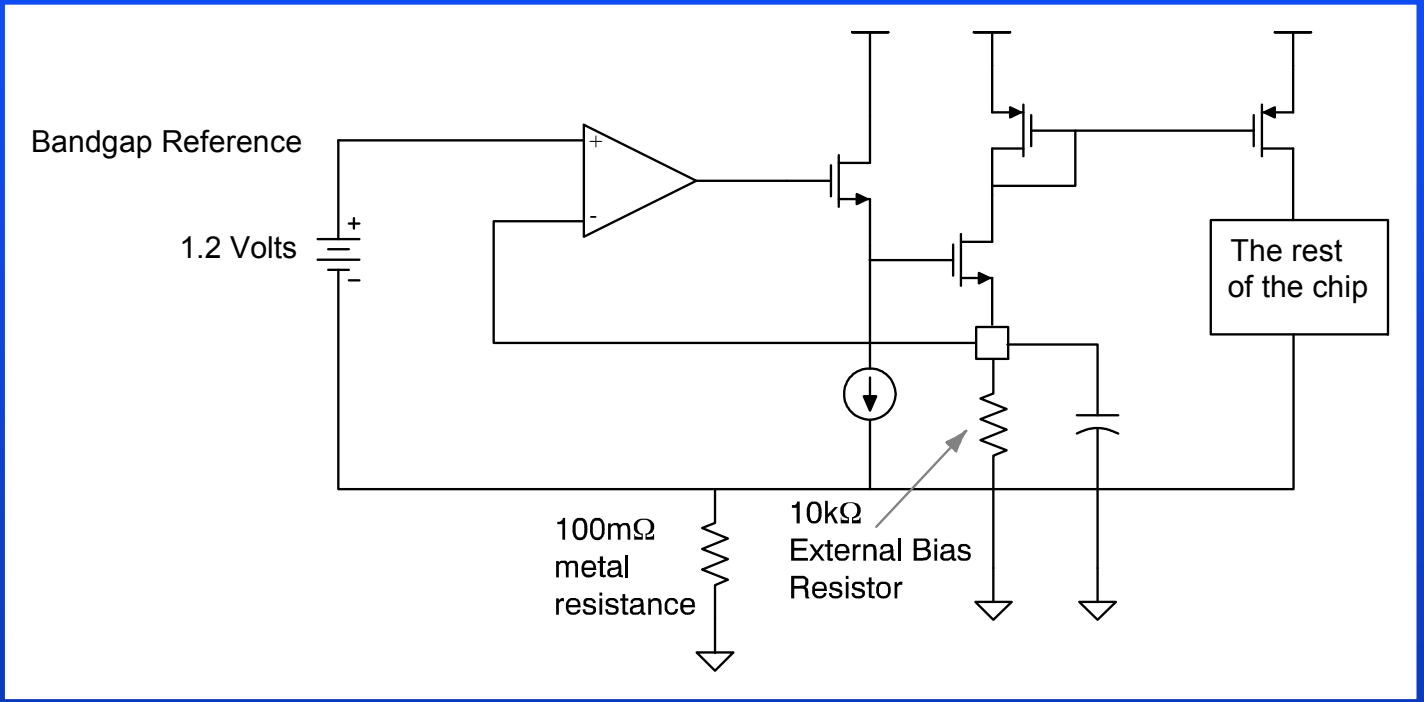
After plastic encapsulation, the fringe extends into plastic ($\varepsilon > 1$, perhaps 3?)

Additional Solution: Metal Shield

- As much of the capacitor area as possible should be covered with metal.
- This caused the fringe fields to terminate on the “shield” (the metal covering) and not on adjacent capacitors. Because this was a single-metal process the coverage was not perfect.
- In today’s multi-metal processes, using one layer as a shield plate is easy.

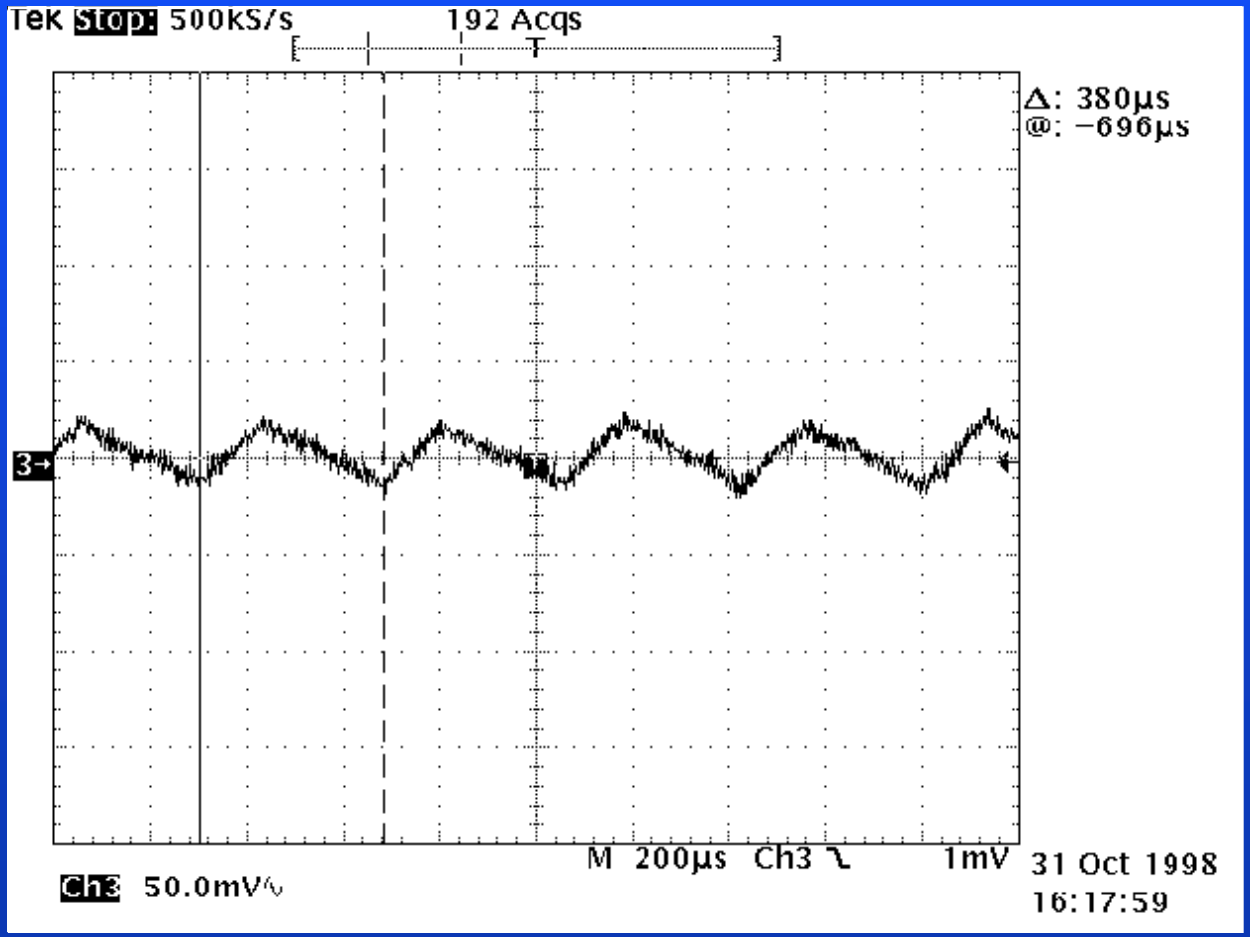
The Whole Chip Oscillates!

The Circuit


Bandgap Reference
1.2 Volts
+
-
+
-
The rest
of the chip
100mΩ
metal
resistance
10kΩ
External Bias
Resistor

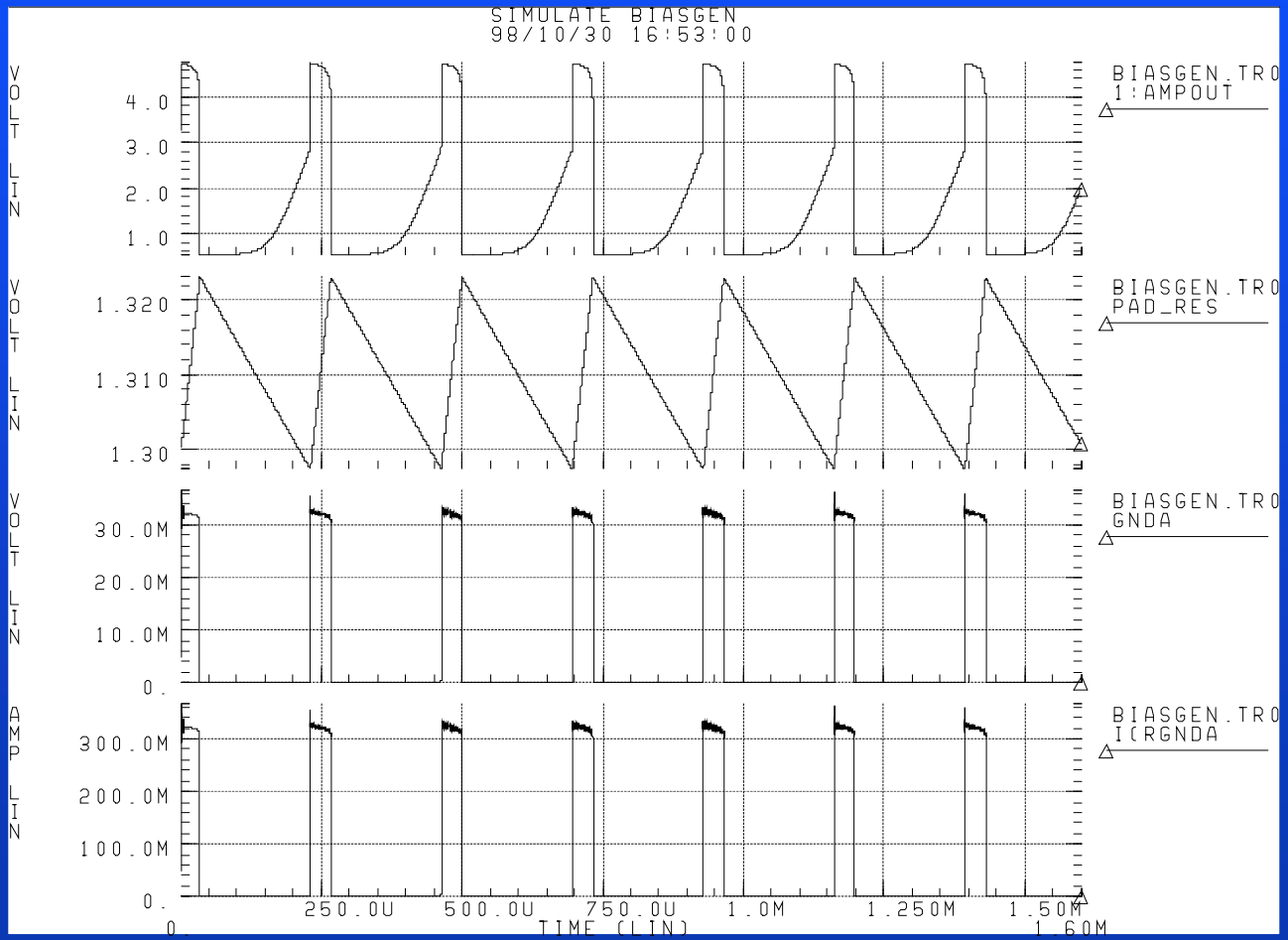
Laboratory Observations

Bias Pin



Spice Simulation

Bias Pin



The Moral of the Story...

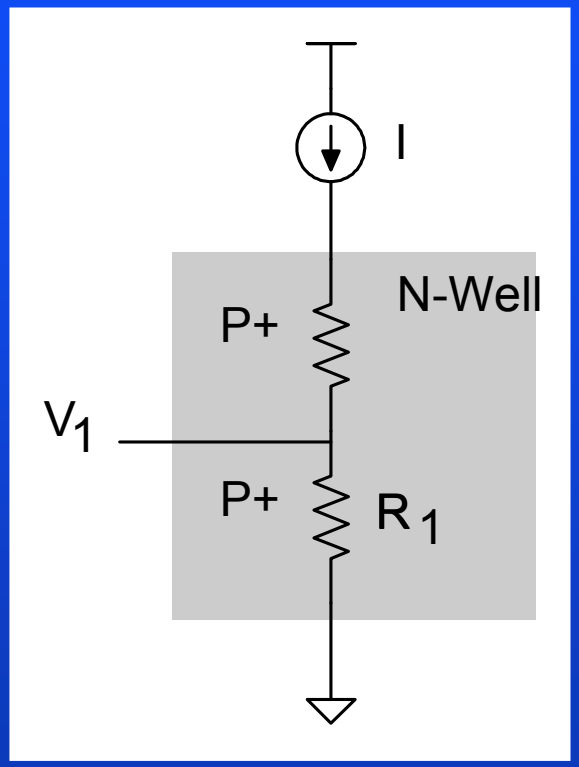
- **Watch out for BIG feedback loops**
- **Dont always ignore 100mΩ of metal**

“You Don’t Miss the Water ‘til the Well Runs Dry”

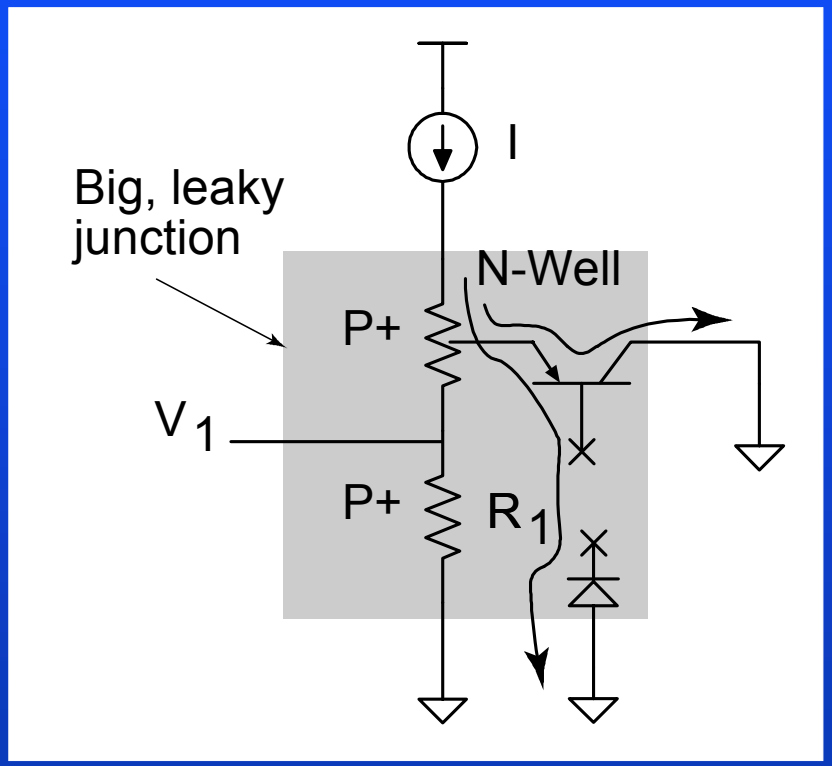
Parasitic Bipolars

- In a Bandgap Reference design, it was discovered that a P+ resistor string was lying inside an N-Well which was floating.
- Is that a problem?

The Circuit (w/o Parasitics)



The Circuit (w/ Parasitics)



Temp. Leakage

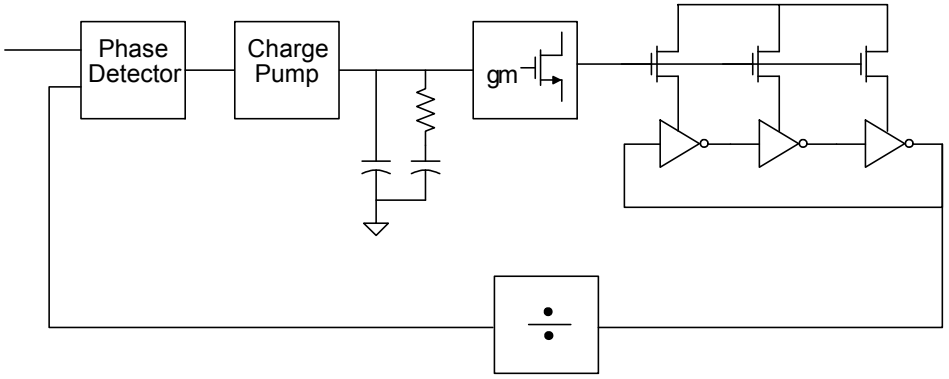
The Moral of the Story

- **Think about where your N-Well is connected.**
- **Use three-terminal resistors!!!**
  - **This forces you to think!**

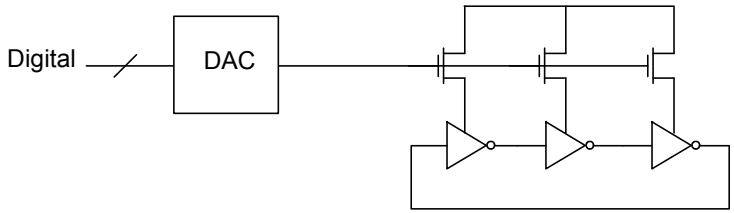
Remember Christian Huygens

Coupled Oscillators

The Circuit

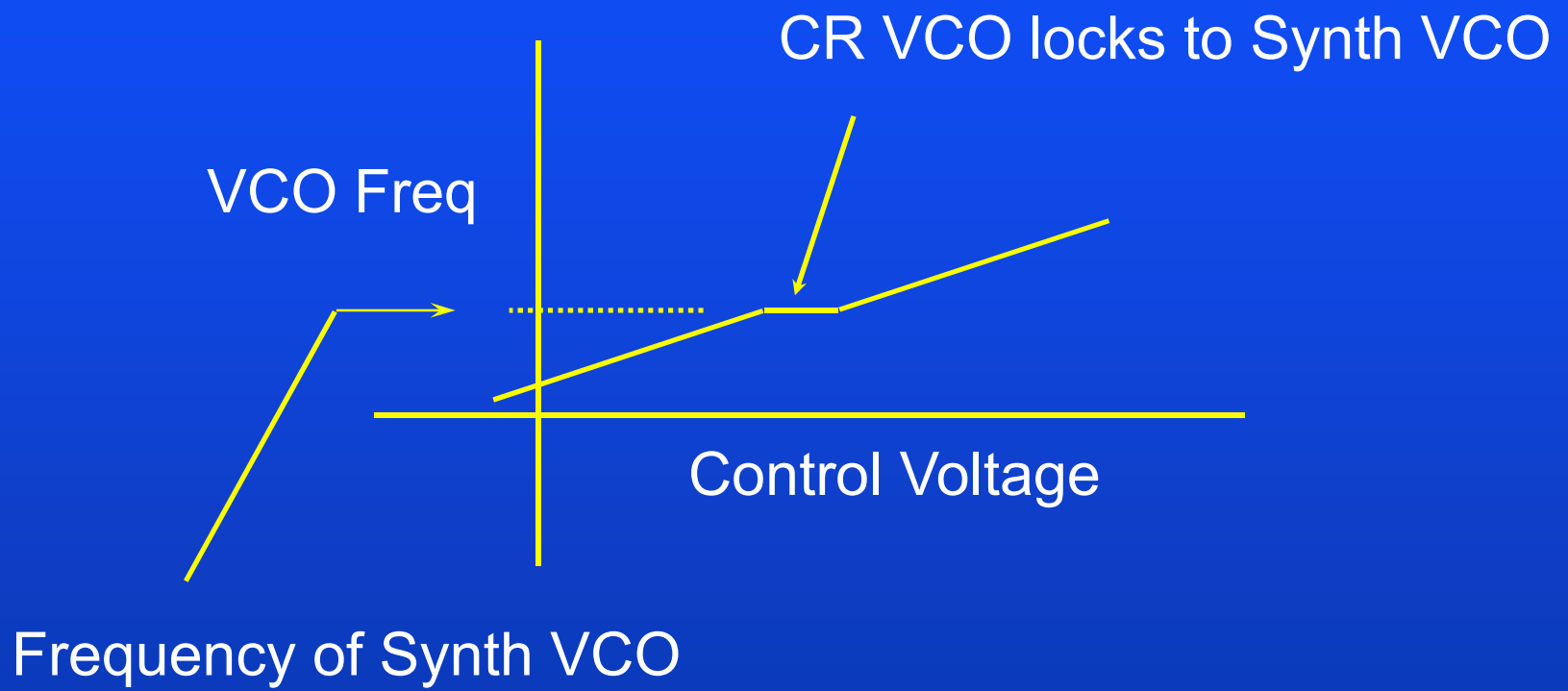


Synthesizer with VCO

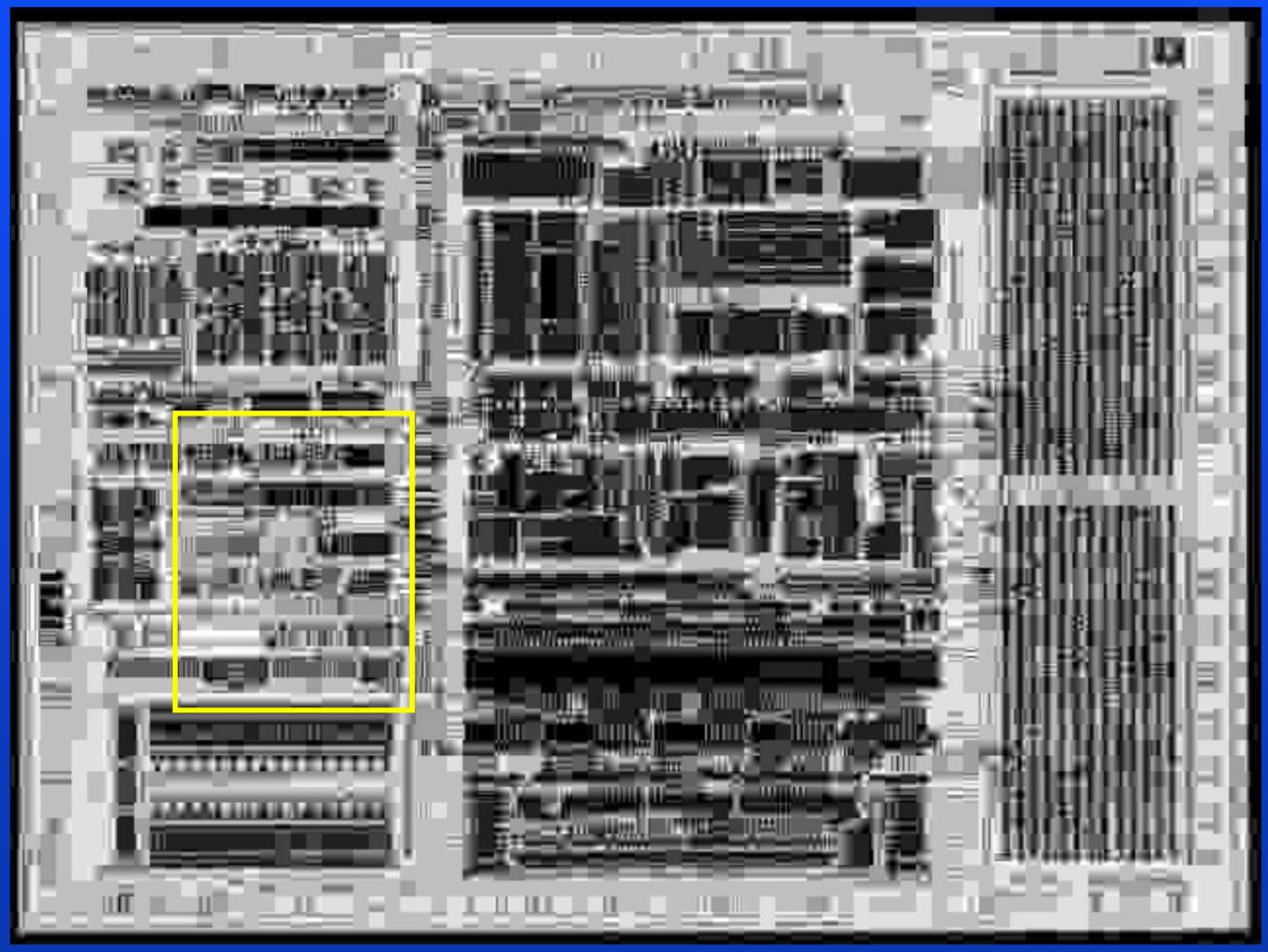


Clock Recovery DAC and VCO

Transfer Function of CR VCO Measured in the Lab

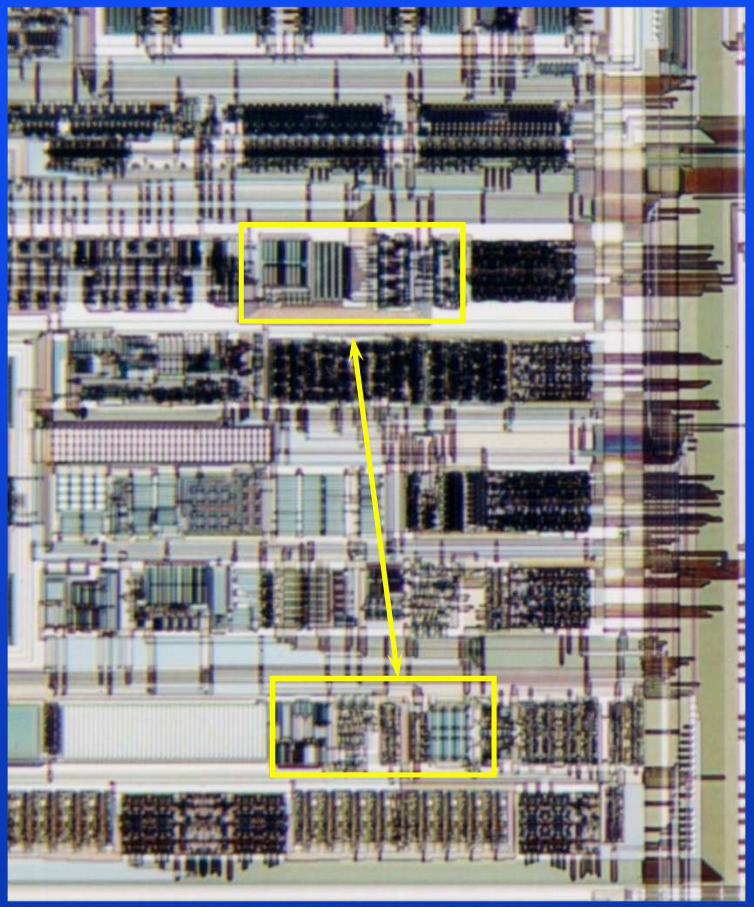


Layout of Two VCOs



Layout Detail

Separation
approx: 1.5mm



Solution

- Separate VCOs with distance
- Reduce substrate coupling path with improved layout

The Clock Experiment

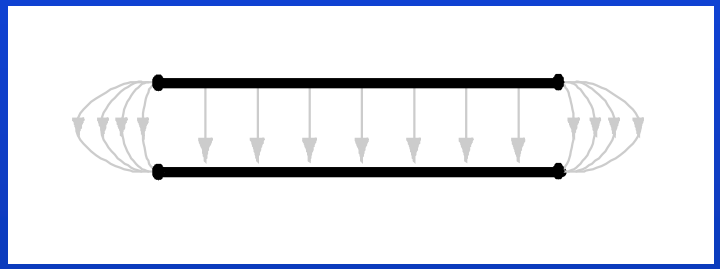
Matching Principles

Matching Principles

- Unit Replication
- Yiannoulos-Path
- Uniform Perimeters
- Avoid hard corners for capacitors
- Common Centroid
- Photolithographic Invariance
- The same means *the same*

Unit Replication Principle

Capacitor Example



Total capacitance has an area and a perimeter component

Perimeter/Area Ratio

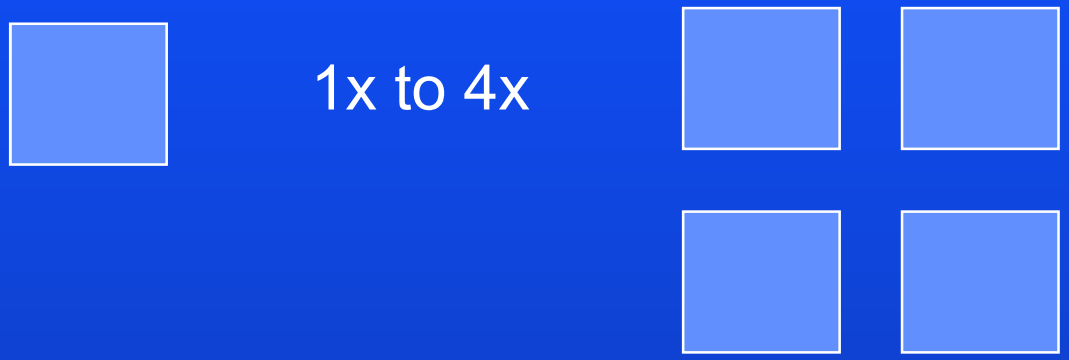
$$C_1 = C_{1A} + C_{1P}$$

$$C_2 = C_{2A} + C_{2P}$$

$$\frac{C_2}{C_1} = \frac{C_{2A} + C_{2P}}{C_{1A} + C_{1P}} = \left[\frac{C_{2A}}{C_{1A}}\right]\left[\frac{1 + \frac{C_{2P}}{C_{2A}}}{1 + \frac{C_{1P}}{C_{1A}}}\right]$$

Match C_P/C_A to force the overall ratio to the area ratio.

Unit Replication



Both areas and perimeters are matched!

1:4 ratio for perimeters, 1:4 ratio for areas

Unit Replication

- **The Unit Replication Principle applies to:**
  - **Capacitors**
  - **Transistors**
  - **Resistors**

USE IT!

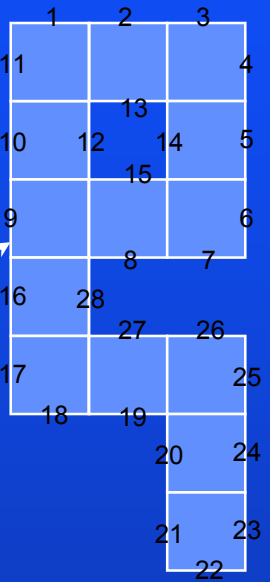
Non-Unit Ratios

- **What do you do if you need a ratio that requires a non-unit ratio?**
  (I.e., What do you do if the size of a unit capacitor for the particular ratio desired is too small to use the unit matching technique.)
- **E.g., 1:4.1; Unit cap is 10fF. You cannot build an 0.1fF cap.**

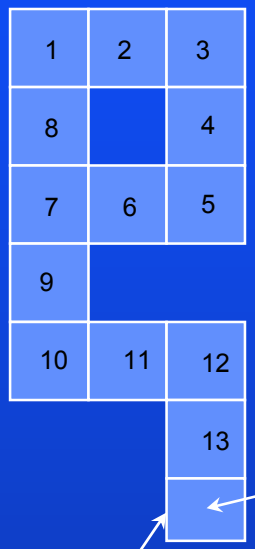
Rule: Don't use "i.e." when you mean "e.g."

Solution: The Yiannoulos[1]-Path Technique

Example: Desired Ratio - 13.8:14



Length of side for one unit=1



Area=0.8 units

Length of side=0.8

Ratio of areas: 14:13.8

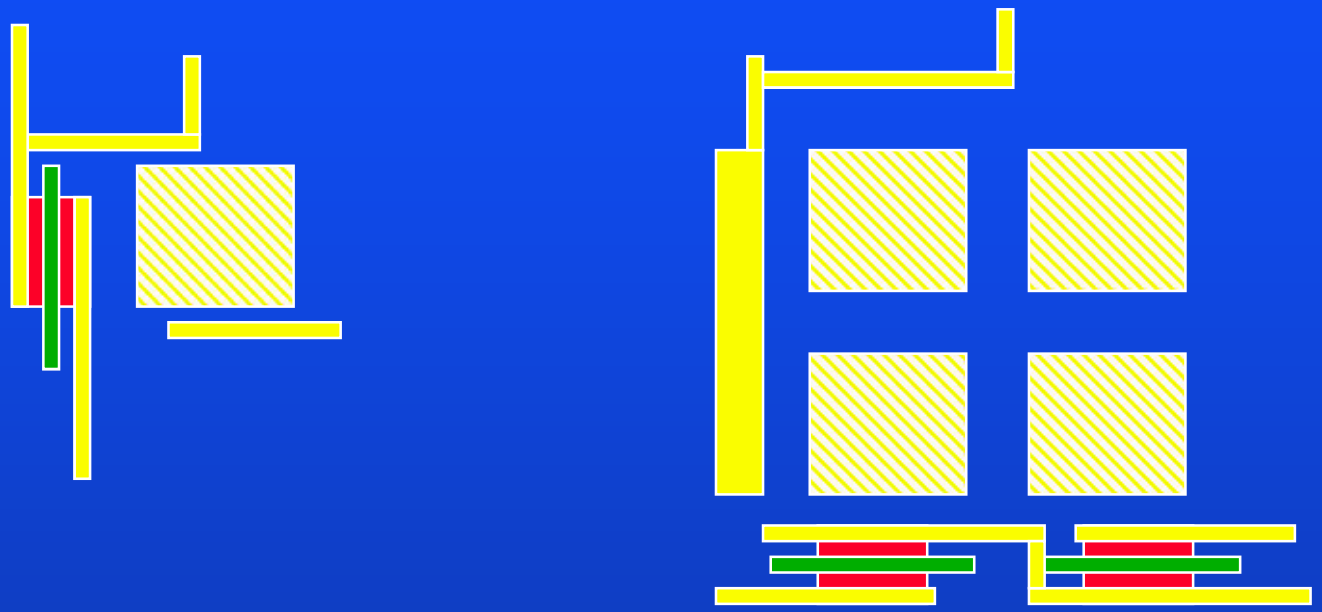
Ratio of perimeters: 28:27.6

Amazing!

1. Aristedes A. Yiannoulos

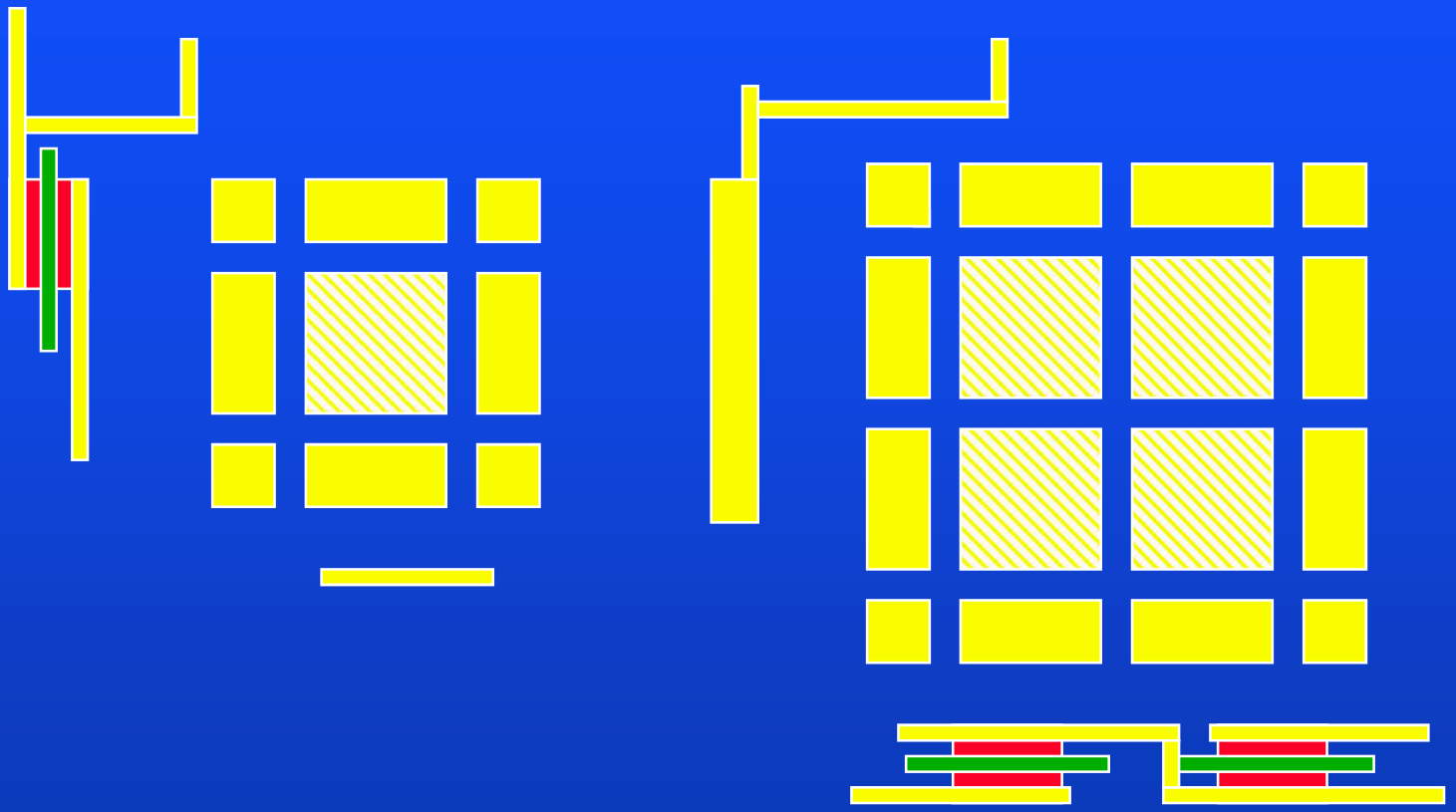
Uniform Perimeter Principle

Capacitor Example



How accurate is the 1:4 ratio given the perimeter difference?

Uniform Perimeter Principle



The perimeter of every unit is the same.

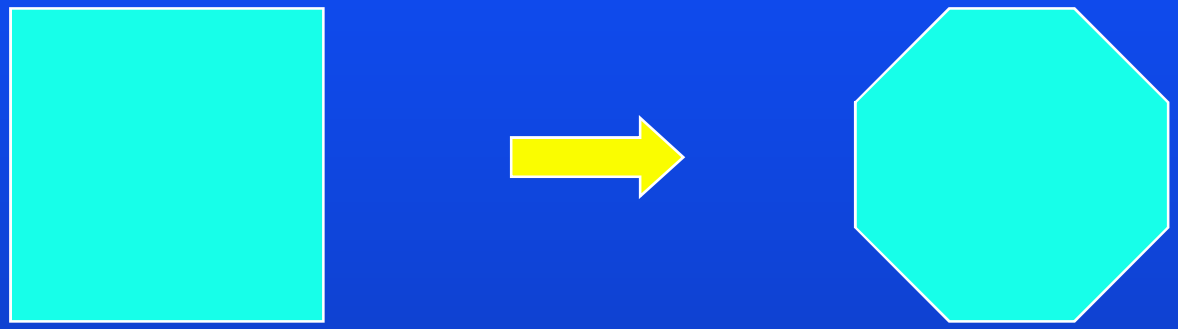
USE IT!

Uniform Perimeter Principle

- **Imagine yourself as being really small.**
- **Stand at the center of a unit component and peer in all directions.**
- **If you cannot determine which unit component you are standing on, then you have properly applied the *Uniform Perimeter Principle.***

How far out do you have to match? Just far enough!

Avoid Hard Corners for Capacitors



Why?

Consider a Circle vs. Square

$$A_{circle} = \pi\ r^2$$

$$A_{square} = d^2$$

$$if\ \ A_{circle} = A_{square}$$

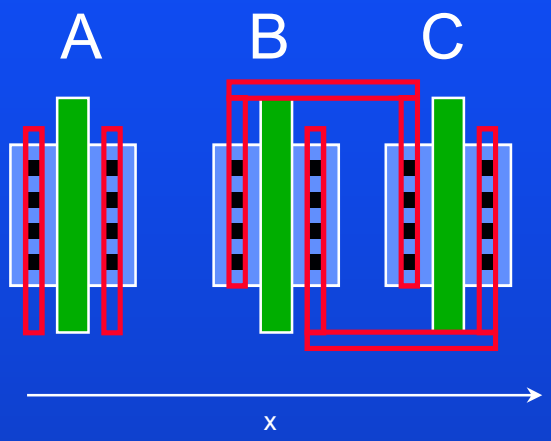
$$r = \frac{d\sqrt{\pi}}{\pi}$$

$$\frac{P_{circle}}{P_{square}} = \frac{2\sqrt{\pi}\ d}{4d} = \frac{\sqrt{\pi}}{2} < 1$$

Perimeter effects are minimized

Common Centroid Principle

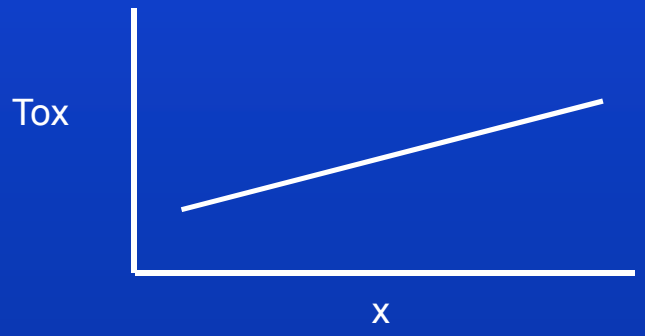
Transistor Example



$V_{TA} < V_{TB} < V_{TC}$

Thus:

$I_{BC} < 2I_A$



Common Centroid Principle

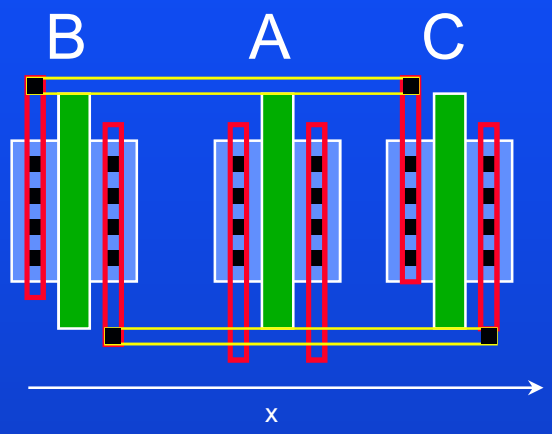
$V_{TB} < V_{TA} < V_{TC}$

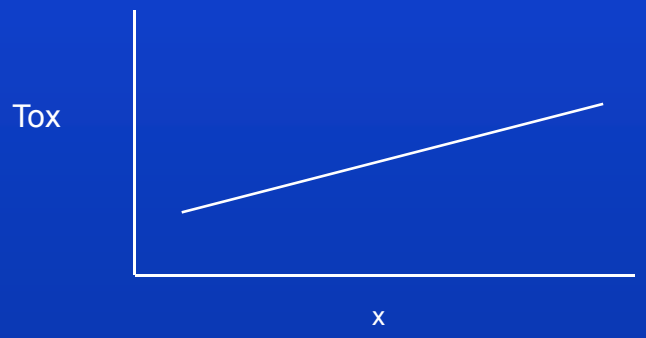
$(1/2)(V_{TC} + V_{TB}) = V_{TA}$

Thus:

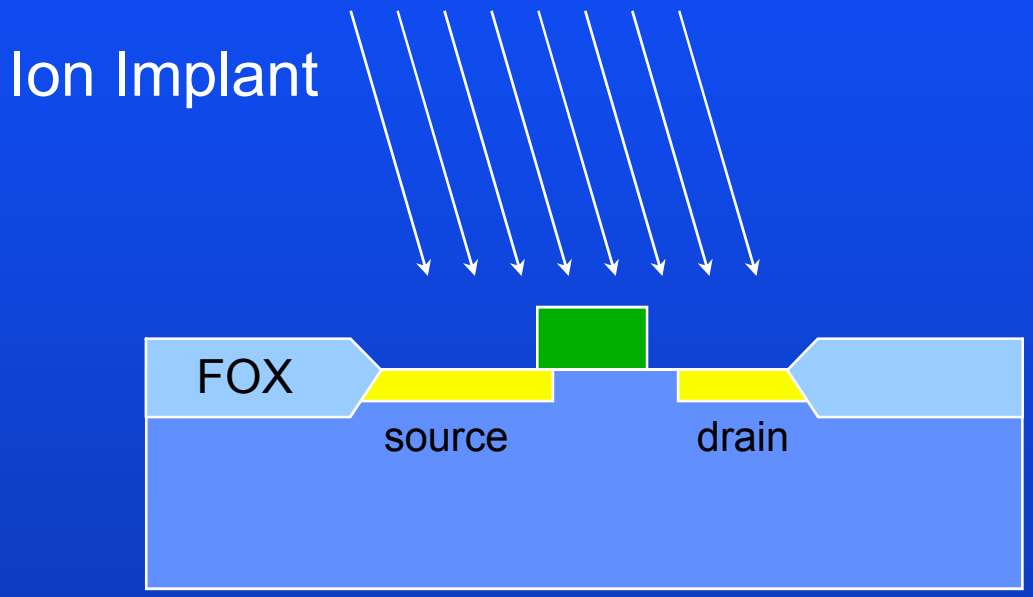
$I_{BC} = 2I_A$

to a first-order approximation



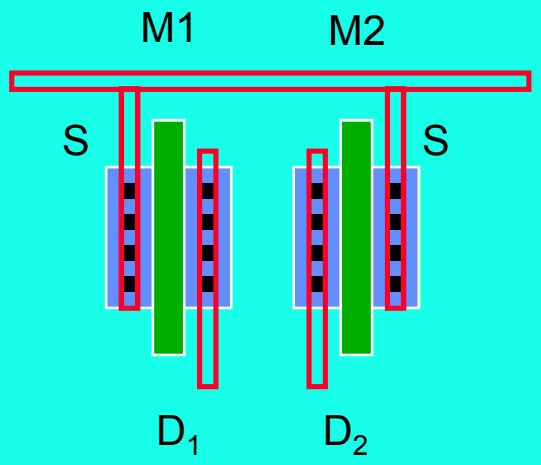


Photolithographic Invariance Principle

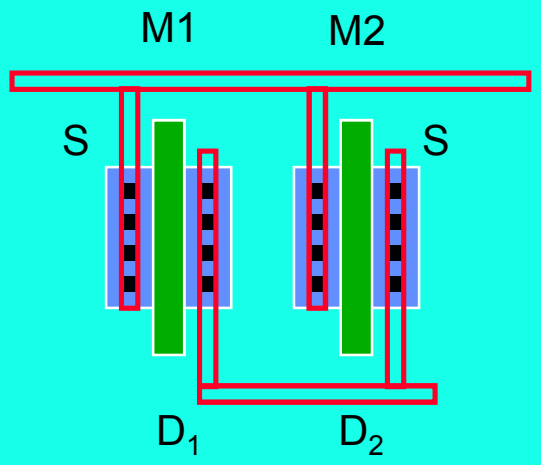


Because of implant angle, polysilicon casts a shadow on to drain/source region.

Photolithographic Invariance Principle



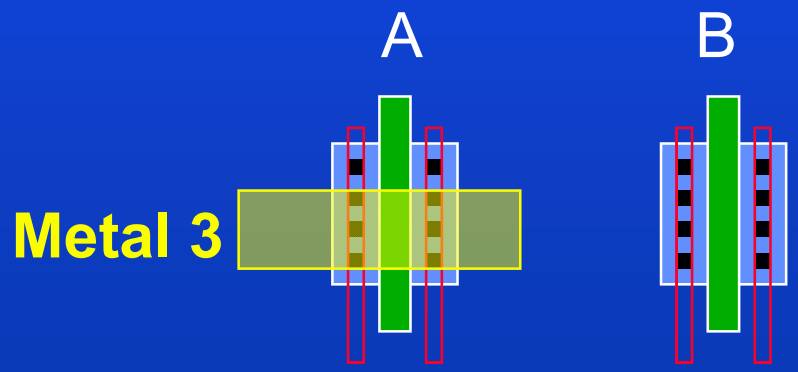
$C_{GD1} < C_{GD2}$



$C_{GD1} = C_{GD2}$

The Same IS The Same

- **Unit matching requires that every aspect of things being matched are the same.**
- **For MOSFETs, this means metal coverage as well!**



Transistors A and B are NOT matched!

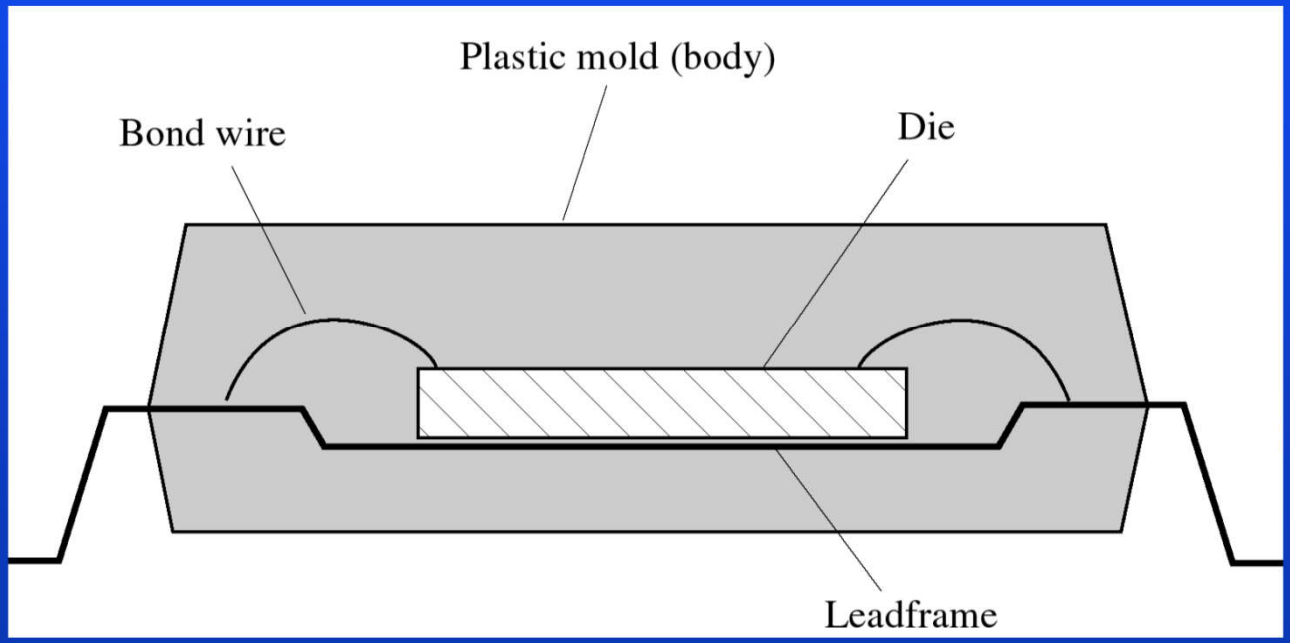
Metal Coverage Issues

- For critical matching, do not cover matching transistors with metal.
- For less critical matching, at least cover the matched transistors in the same way.

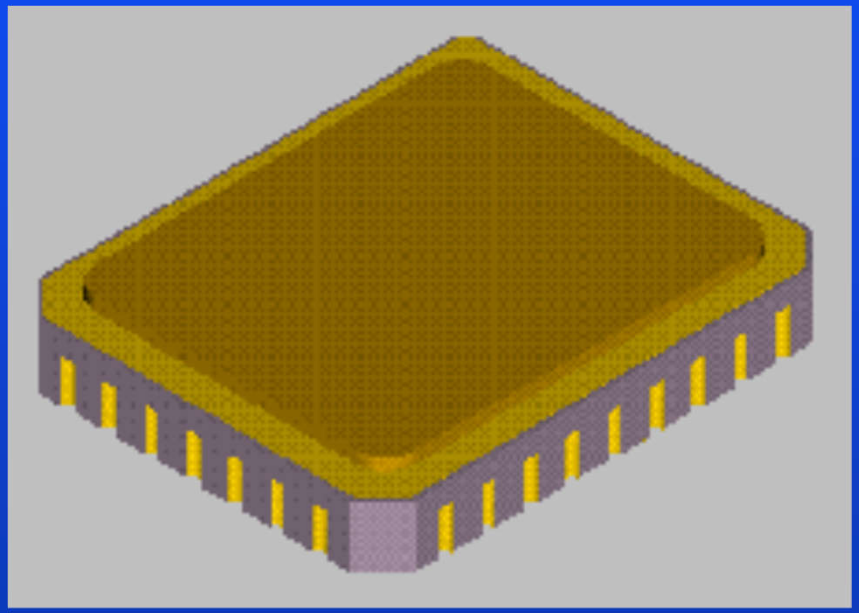
Package Parasitics

Picking Proper Package Pinout

Typical Plastic Package Cross Section



LCC Package



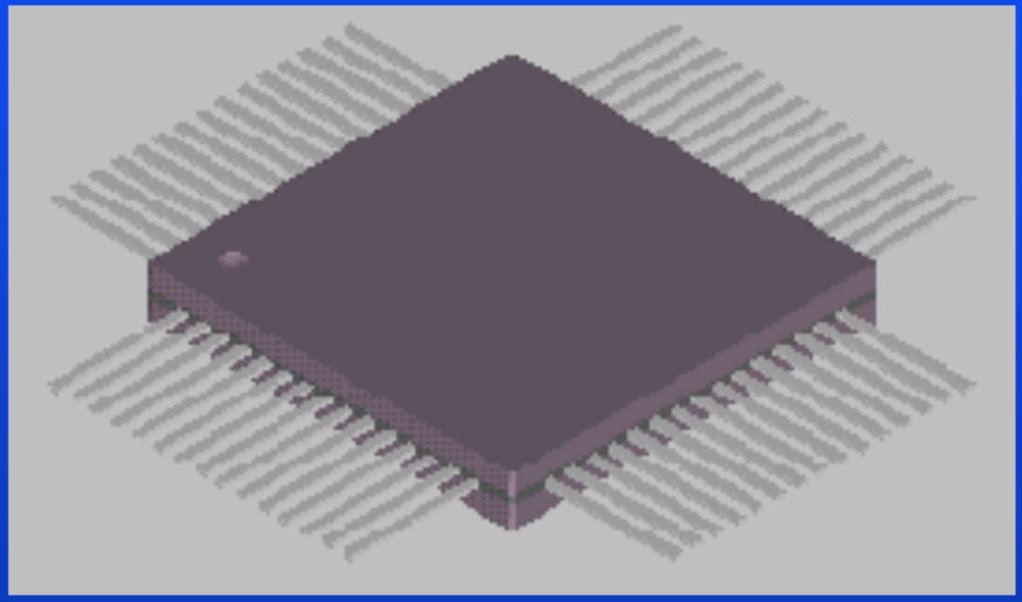
LCC Package Parasitics

LCC Package Data

Lead Count	Electrical parameter			
	R (mΩ)	L (nH)	C_L (pF)	C_{LL} (pF)
20 square	68 - 78	3.5 - 6.3	0.8 - 0.9	0.3 - 0.4
28 square	68 - 78	3.7 - 7.8	1.0 - 1.1	0.4 - 0.5
28 rectangle	68 - 78	3.3 - 4.2	0.6 - 0.7	0.2 - 0.3
32 rectangle	68 - 78	3.9 - 5.8	0.8 - 1.1	0.1 - 0.6
44 square	68 - 78	4.3 - 6.1	1.1 - 1.4	0.2 - 0.8
52 square	68 - 78	6.1 - 8.4	1.0 - 1.3	0.2 - 0.8
68 square	68 - 78	5.3 - 8.9	1.4 - 2.0	0.2 - 1.0
84 square	68 - 78	8.4 - 10.8	1.8 - 2.7	0.25 - 1.2

Note: C_L is load capacitance and C_{LL} is lead-to-lead capacitance

QFP Package



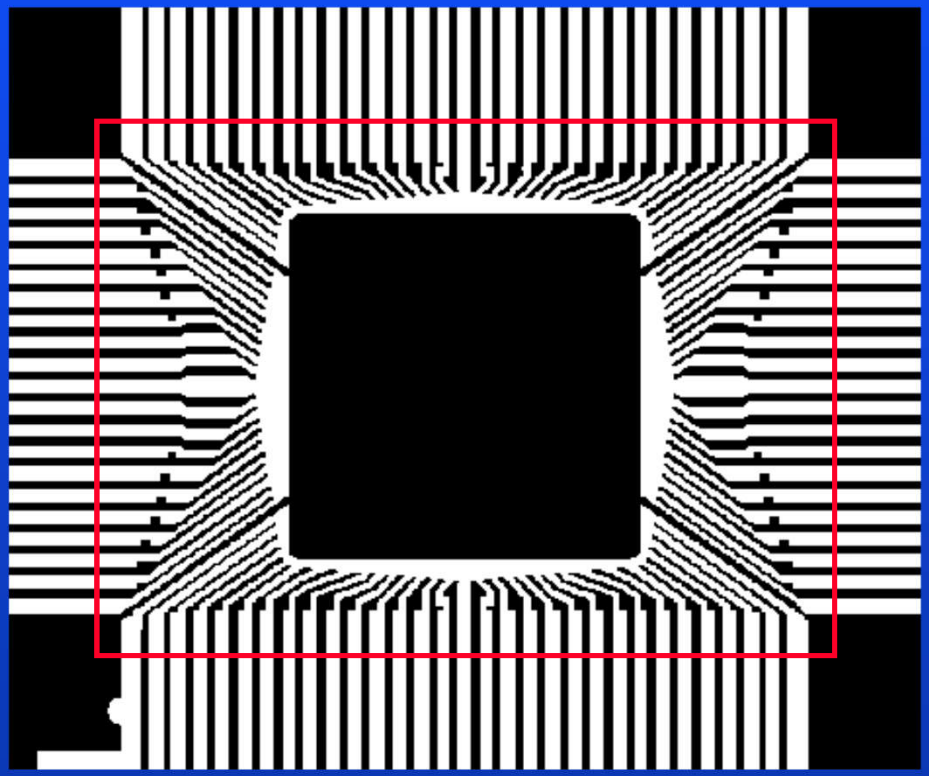
QFP Package Parasitics

QFP Package Data

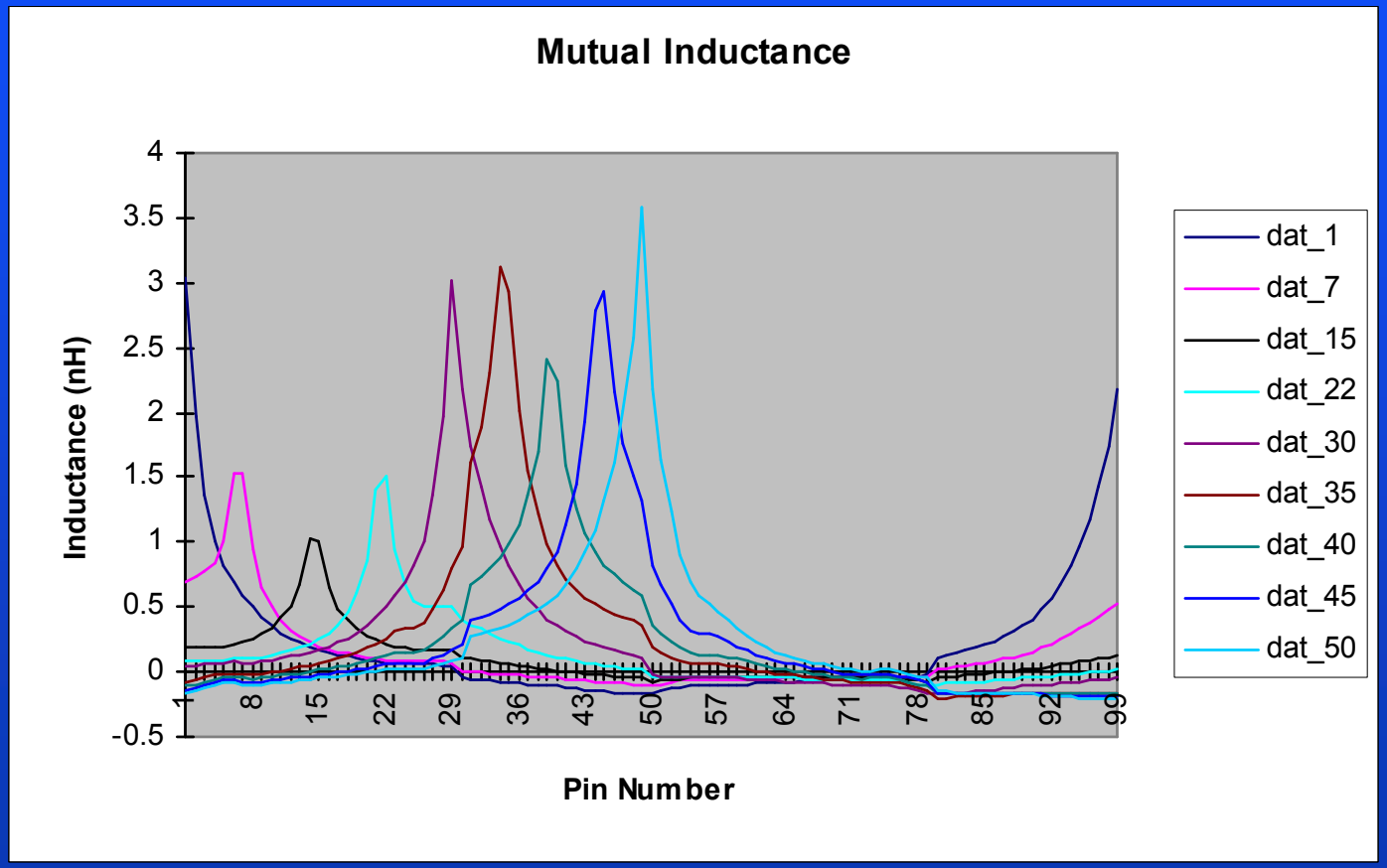
Lead Count	Electrical parameter			
	R (mΩ)	L (nH)	C_L (pF)	C_{LL} (pF)
84	70-80	5.8 - 6.6	< 1.0	< 0.5
100	70-80	6.1 - 7.1	< 1.5	< 1.0
132	70-80	7.3 - 8.5	< 2.0	< 1.5
164	70-80	8.0 - 14.5	< 2.2	< 1.5
196	70-80	9.0 - 15.5	< 1.5	< 1.6

Note: C_L is load capacitance and C_{LL} is lead-to-lead capacitance

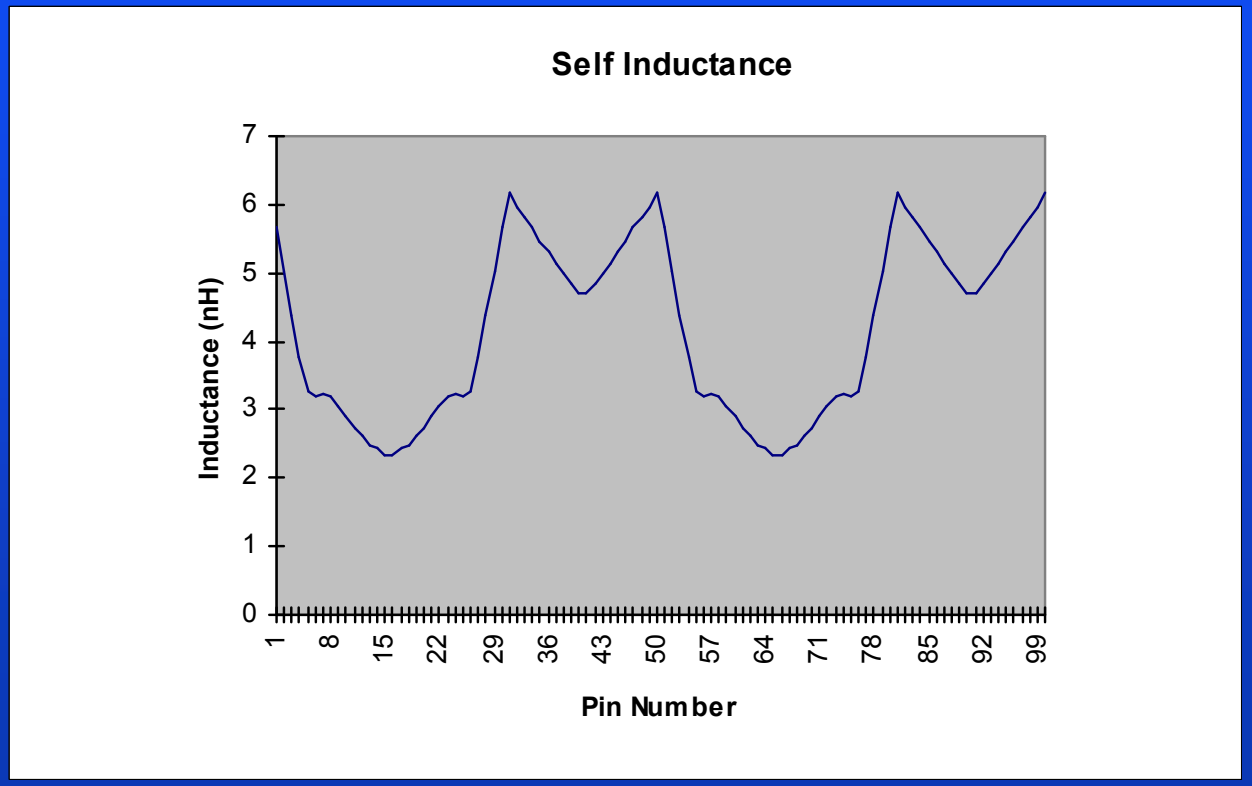
Typical QFP Leadframe



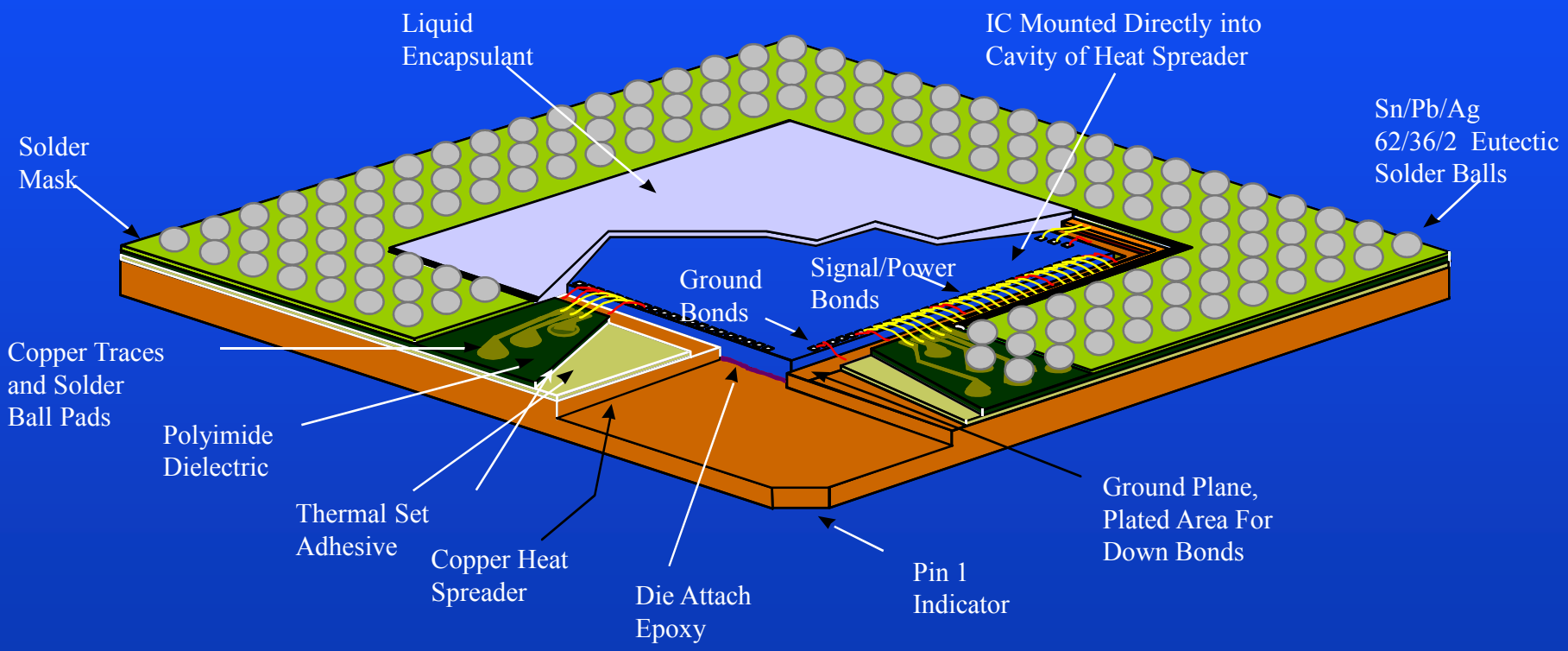
PQFP Pin-Pin Mutual Inductance



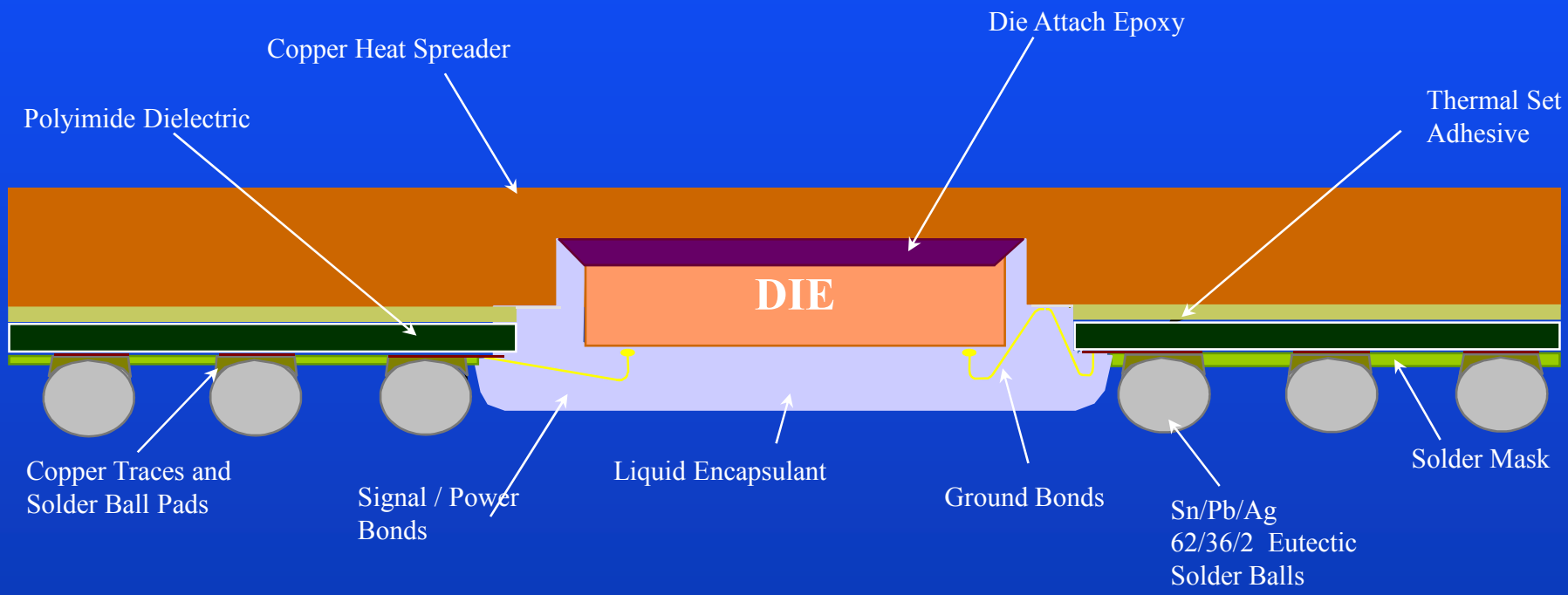
PQFP Self Inductance



TBGA CONSTRUCTION



TBGA



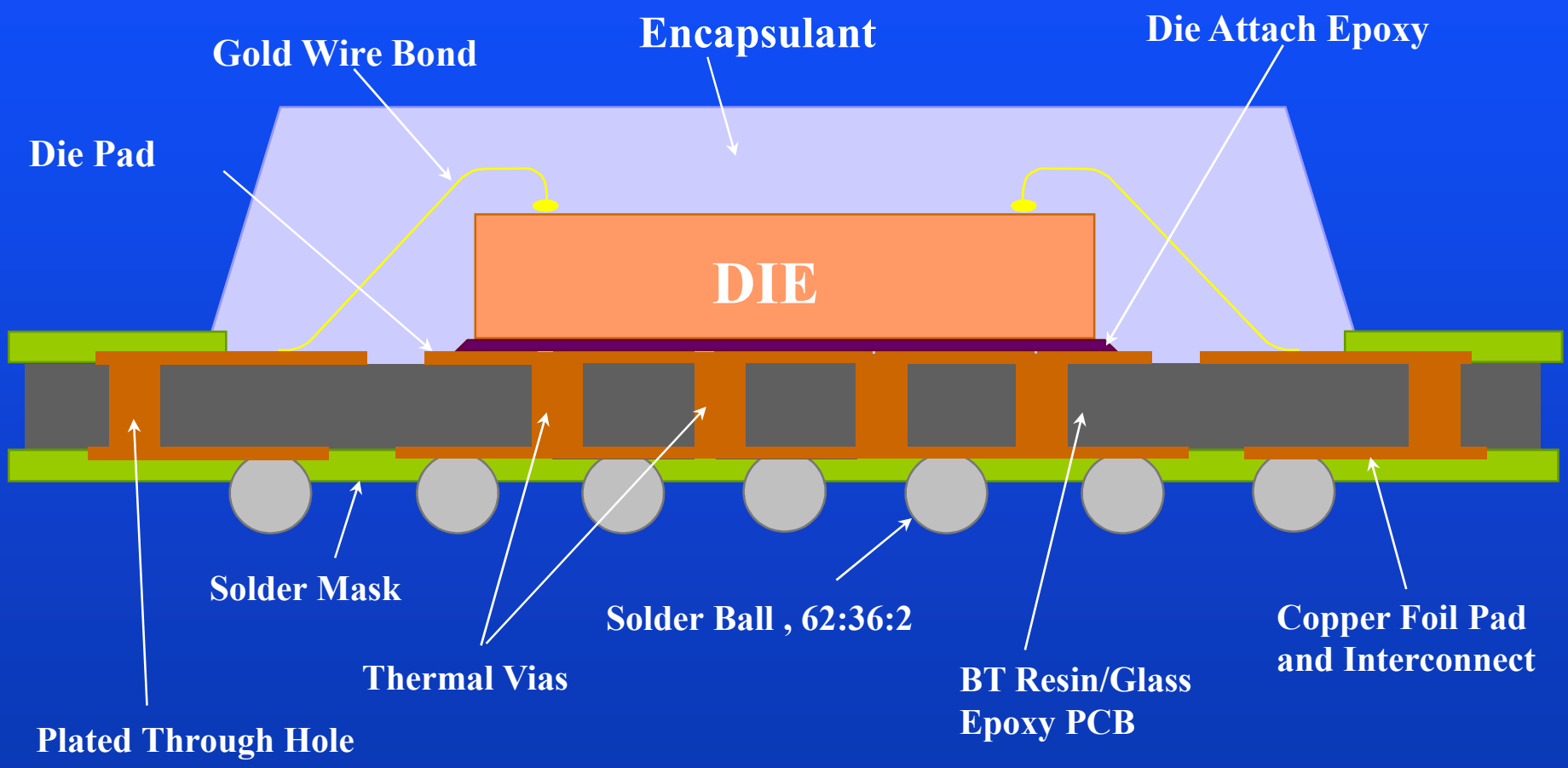
NOT TO SCALE

TBGA vs PBGA
ELECTRICAL COMPARISON
Measured and Modeled Data

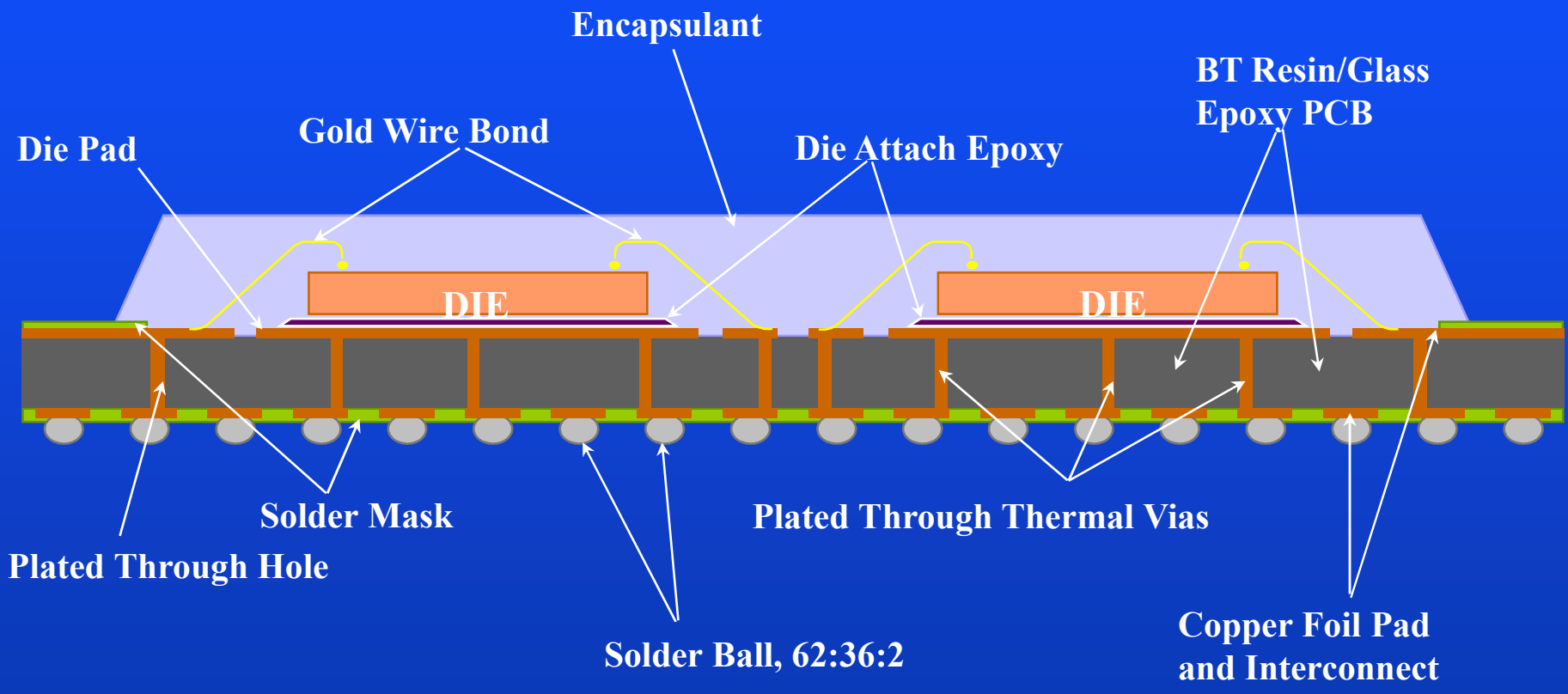
	INDUCTANCE (nH)				CAPACITANCE (pF)			
	Corner		Center		Corner		Center	
	L11	L12	L11	L12	C11	C12	C11	C12
256 PBGA								
■ Measured	6.4	0.3	1.8	0.3	1.1	<0.1	0.7	<0.1
■ Modeled	6.5	0.4	2.0	0.8	1.0	<0.1	0.4	<0.1
256 TBGA								
■ Measured	9.0	3.0	3.5	1.2	1.0	0.5	0.9	0.3
■ Modeled	9.1	2.5	3.7	1.3	1.0	0.3	0.9	0.1
352 TBGA								
■ Measured	10.0	2.0	3.6	0.8	1.3	0.2	1.1	0.1
■ Modeled	10.4	2.1	3.4	0.9	1.0	<0.1	0.4	<0.1

*256=27x27mm / **352=35x35mm

PBGA DESIGN


Gold Wire Bond
Encapsulant
Die Attach Epoxy
Die Pad
DIE
Solder Mask
Thermal Vias
Solder Ball , 62:36:2
Copper Foil Pad
and Interconnect
Plated Through Hole
BT Resin/Glass
Epoxy PCB
NOT TO SCALE

PBGA MULTI-CHIP MODULE



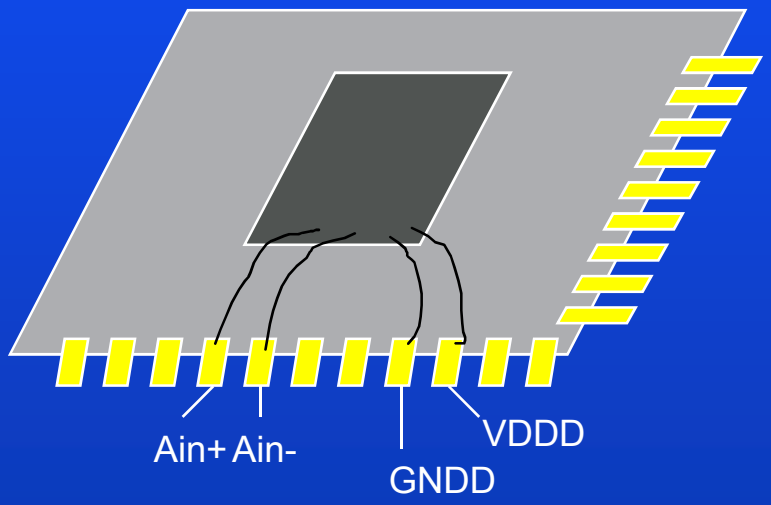
NOT TO SCALE

Minimize Sensitivity to Package Inductance

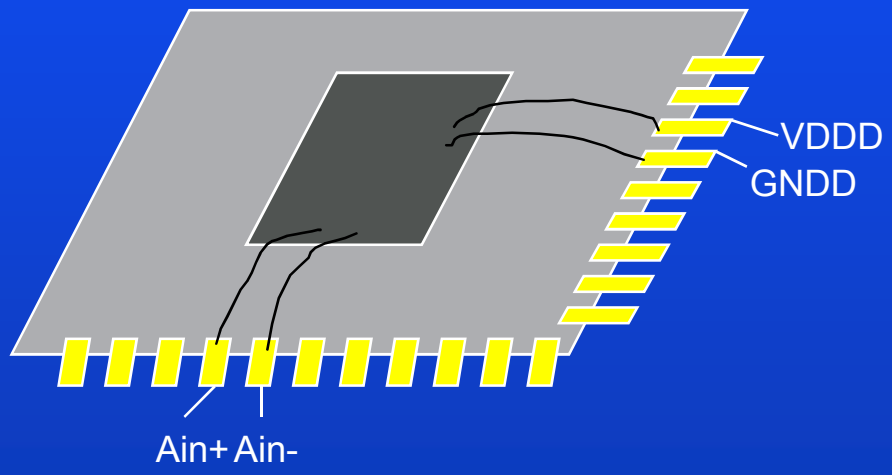
- Take advantage of orthogonality.
- Keep noisy digital currents in pins far away from sensitive analog input pins.
- Use shortest pins for circuits requiring lowest inductance.
- Force opposing loop currents

Take Advantage of Orthogonality

BAD



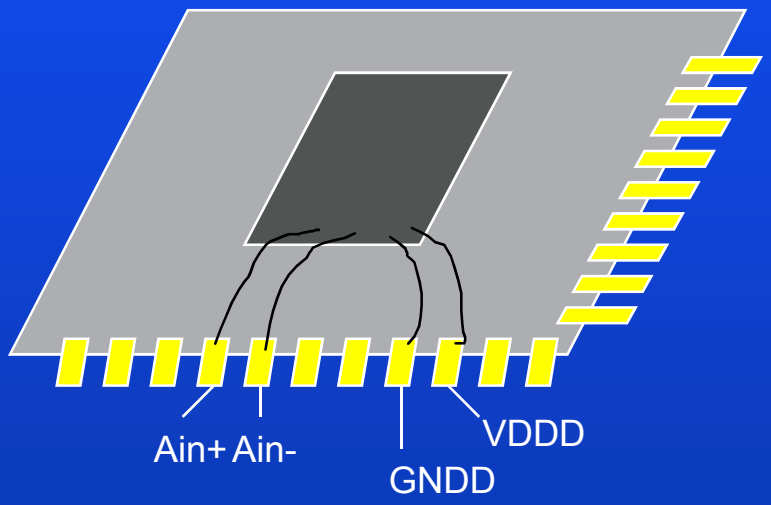
GOOD



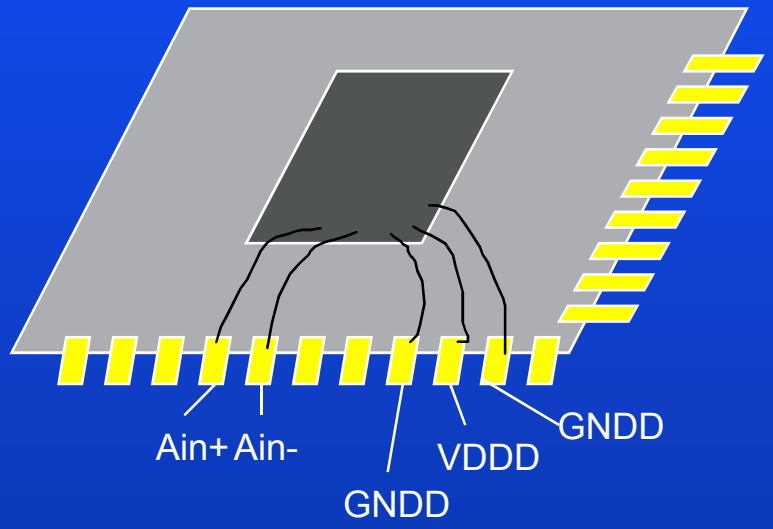
In most cases you are probably OK to place offending pins on opposite sides of the package if the package is large enough.

Force Opposing Currents

BAD



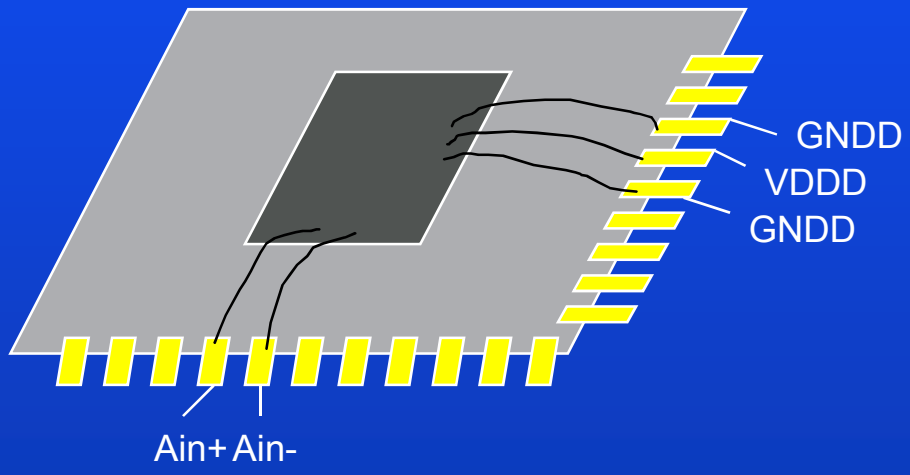
BETTER



Opposing loops cancel

Force Opposing Currents

BETTER YET



Orthogonality plus opposing currents

THE END